Содержание

DCDC

Load Line

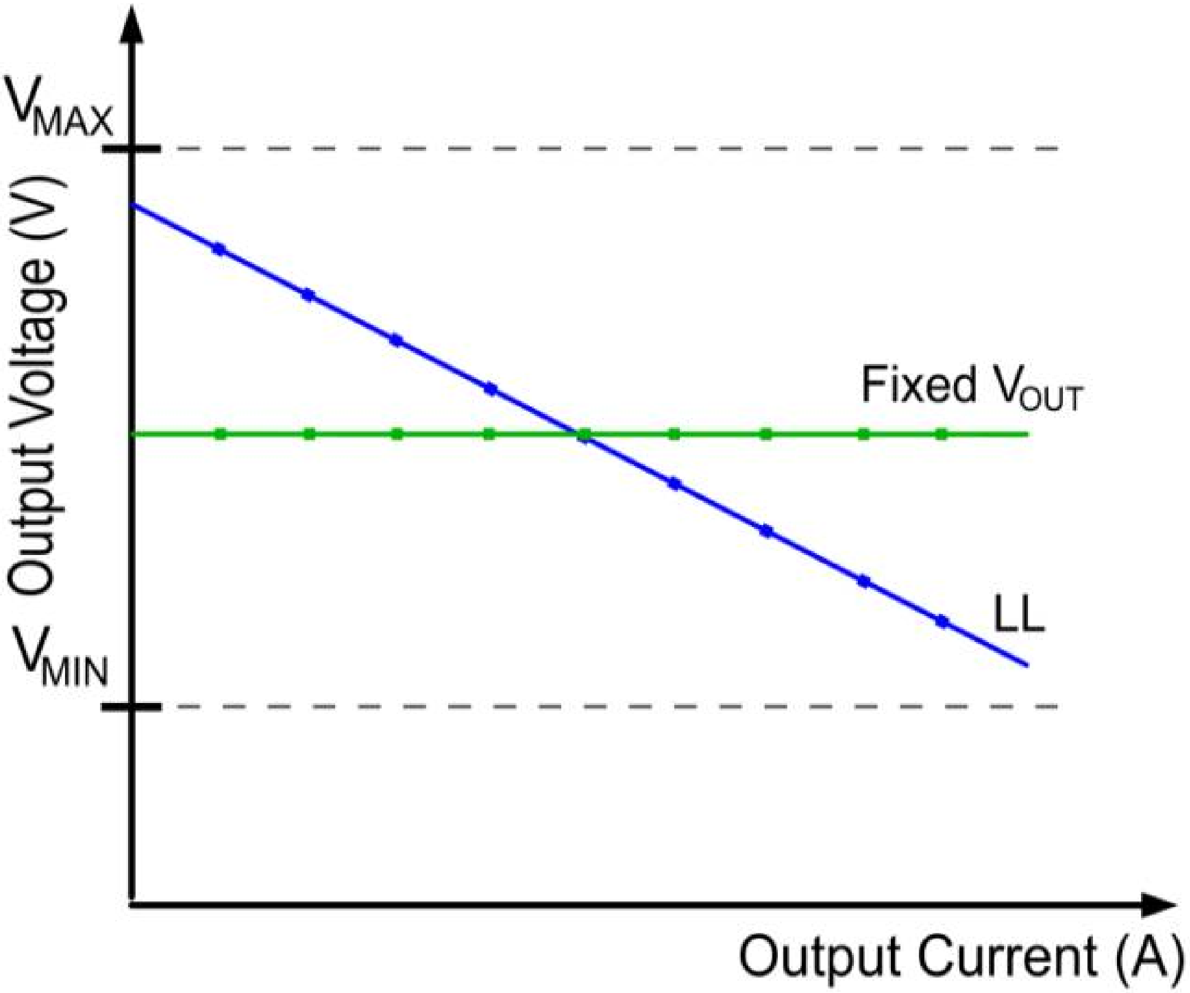


Figure 1: V_{OUT} with DC Load Line vs. the Fixed V_{OUT} Method

https://doc.inmys.ru/hash/cab9b5440d4a49a3630d42354300008e/load-line_design_for_a_multi-phase_buck_converter_r1.0.pdf
https://doc.inmys.ru/hash/a290a7033d13d866a335dc45bea88c7c/Infineon-DCDC_FPGA_load-line-AN-v01_00-EN.pdf

Snubber

Snubber - цепочка, компенсирующая паразитные L и C в DCDC.

- Резистор может прилично греться
- Надо подбирать экспериментально

Про snubber:

- ROHM AN

- Toshiba AN
- Nexperia AN
- TI AN
- Infineon AN

Snubber:

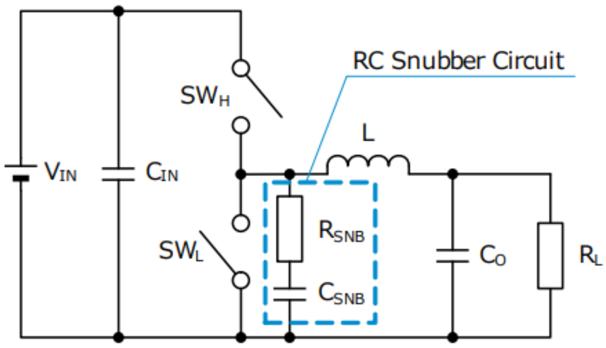


Figure 4. RC snubber circuit

Пример без snubber:

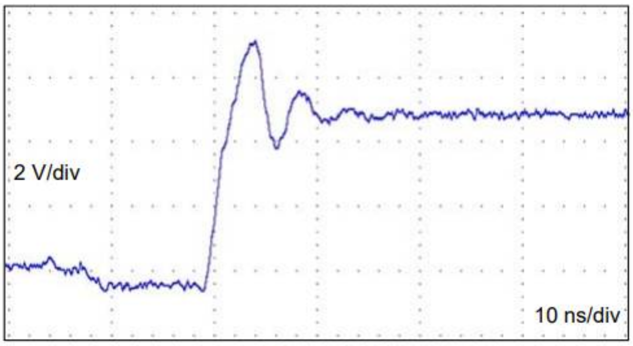


Figure 10. Without snubber circuit

Пример после настройки Snubber:

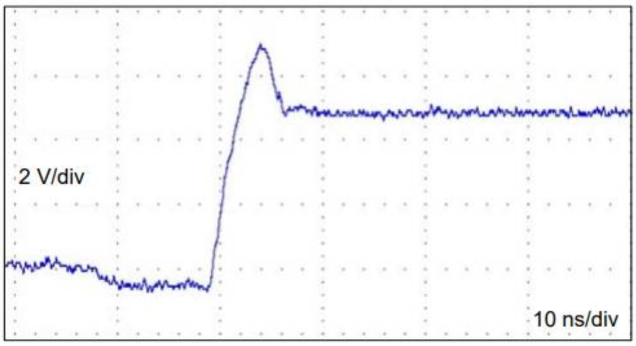


Figure 13. R_{SNB}=3.3Ω, C_{SNB}=680 pF

MOSFET Self-Turn-On Phenomenon

Эффект произвольного включения верхнего транзистора.

Про эффект:

- Toshiba AN

Из app note toshiba:
Selecting MOSFETs with a **high Vth** and a **low Cgd** is of primary importance.

Из даташита ISL6625A:
Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self-coupling via the internal CGD of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor (RUGPH) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage’s rate of rise, the CGD/CGS ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower CDS/CGS ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not affecting normal performance and efficiency.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \qquad \textbf{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. Figure 6 provides a visual reference for this phenomenon and its potential solution.

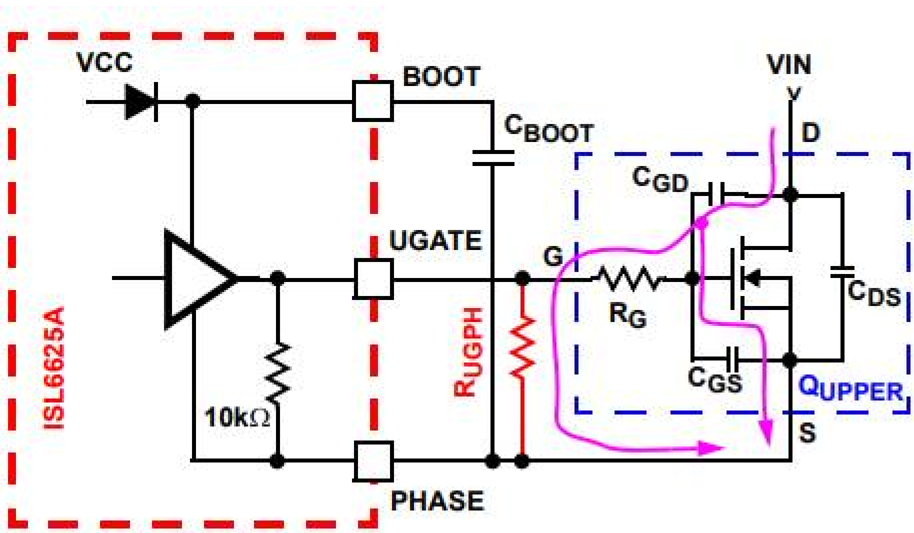
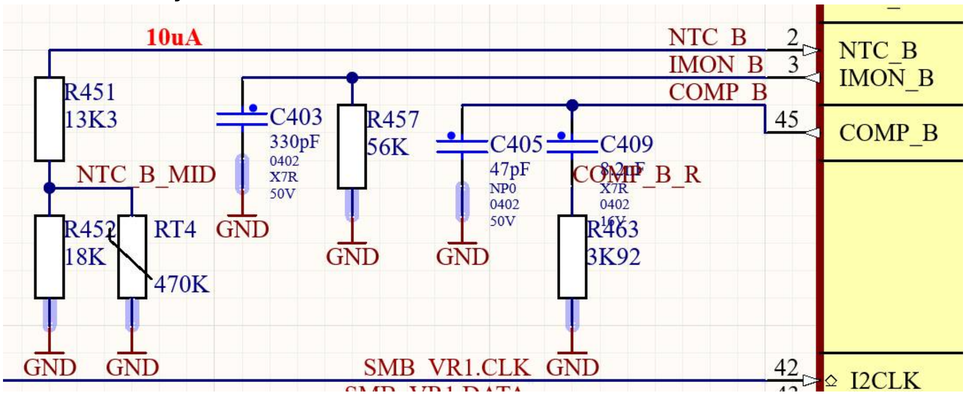


FIGURE 6. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

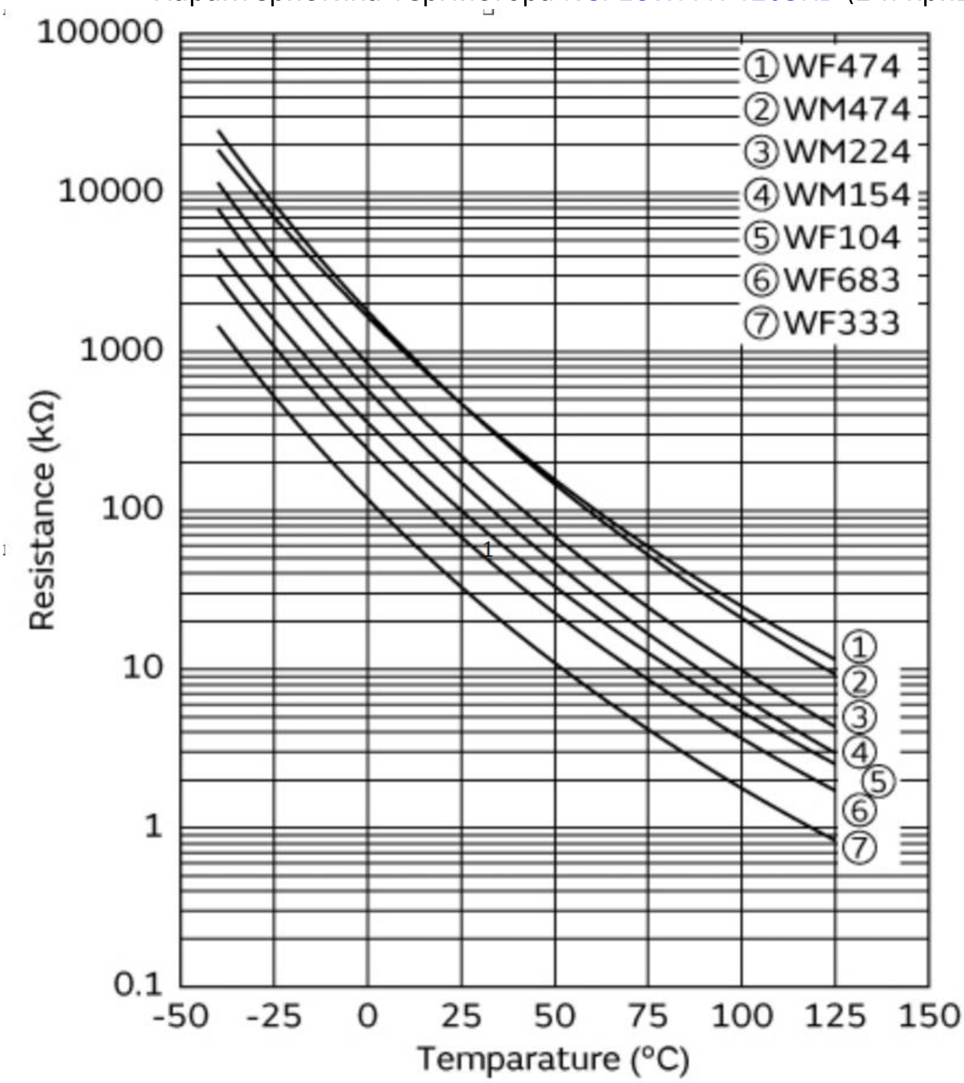
NTC temp measurement and treshold

На примере ISL95866.

Кусок схемы:



Характеристика термистора NCP18WM474E03RB (2-я кривая):



Внутри контроллера:

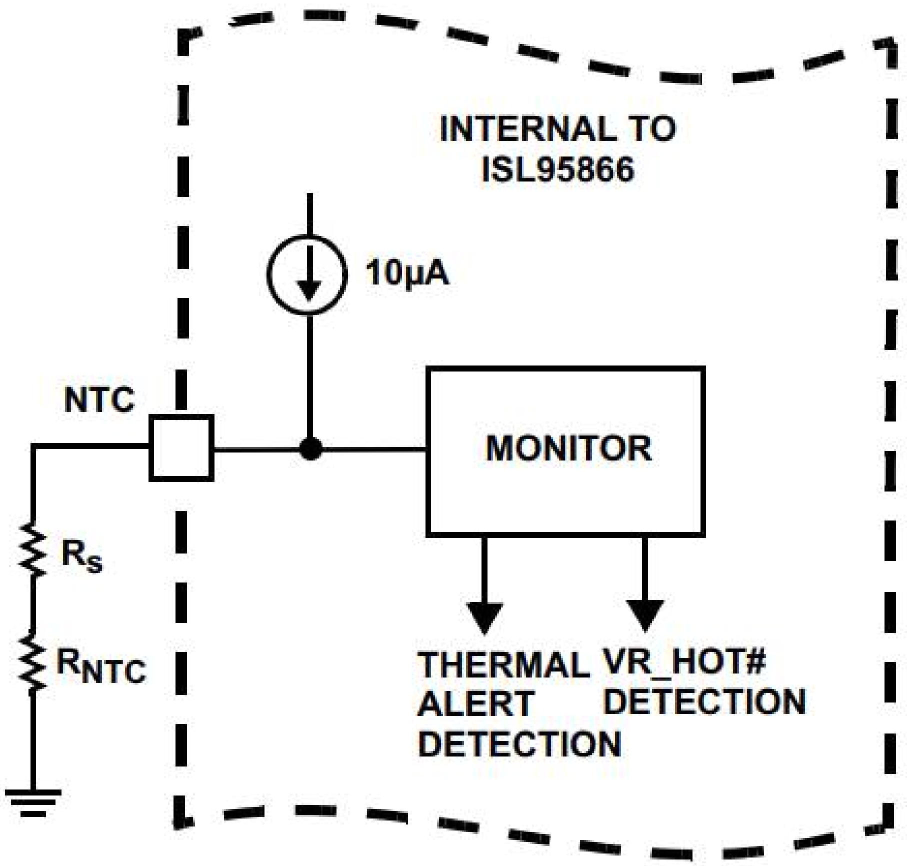


FIGURE 43. NTC CIRCUITRY

Пороги контроллера:

NTC Source Current		NTC = 1.3V	**9.5**	10.0	**10.5**	µA
NTC VR_HOT# Trip Voltage		NTC voltage forced, voltage falling threshold	**0.189**	0.199	**0.209**	V
NTC VR_HOT# Reset Voltage		Rising	**0.211**	0.221	**0.231**	V
Therm_ Alert Trip Voltage		Falling	**0.203**	0.213	**0.223**	V
Therm_ Alert Reset Voltage		Rising	**0.226**	0.236	**0.246**	V

R|| = 1/(1/18k + 1/Rntc)

U = 10uA * (13k3 + R||)

Температура	Сопротивление термистора	Напряжение на входе при токе 10uA
25 град	475k	306mV
75 град	54k	268mV
90 град	25k	237mV

Видно, что при 90 град. защита ещё не сработает.

Если необходимо, чтобы при 90 град. срабатывла защита, то R451 можно заменить на 10K. Тогда получается:

Температура	Сопротивление термистора	Напряжение на входе при токе 10uA
25 град	475k	273mV

Температура	Сопротивление термистора	Напряжение на входе при токе 10uA
75 град	54k	235mV
90 град	25k	204mV

Т.е. при достижении 90 град. будет вырабатываться сигнал VR_HOT. При остывании до 75 град. VR_HOT будет сбрасываться.

Надо всё это проверить.