Содержание

PCIe 3
Docs 3
Connectors 3
Xilinx 4
Artix Ultrascale+ 4
SMARC 4
LTSSM 4

PCIe

Page	Abbreviation	Description	Tags
ltssm	STSSM	Link Training and Status State Machine	pcie

Docs

https://xilinx.github.io/pcie-debug-kmap/pciedebug/build/html/docs/PCIe_Collaterals/index.html	PCIE DEBUG (GENERAL)
https://support.xilinx.com/s/article/56616?language=en_US	56616 - 7 Series Integrated Block for PCI Express - Link Training Debug Guide
https://support.xilinx.com/s/article/73361?language=en_US	73361 - Xilinx PCI Express Gen3 Link Training Debugging Guide for UltraScale and UltraScale+ Devices
https://support.xilinx.com/s/article/71355?language=en_US	71355 - Vivado ILA Usage Guide for UltraScale FPGA Gen3 Integrated Block for PCI Express
https://support.xilinx.com/s/article/1097525?language=en_US	Debugging PCI Express Link Training Issues with Integrated Debugging Features in the IP
https://github.com/Xilinx/chipscopy/tree/master	ILA, JTAG, DDR, PROGRAM

Connectors

Xilinx

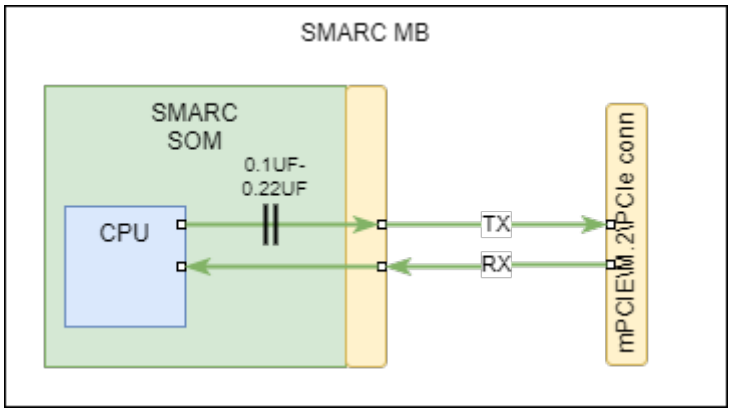
Artix Ultrascale+

PCIe корка стартует нормально только если прошивка быстро загружается из флешки.

Вариант конфигурации через JTAG, а потом ребут компа или пауза в u-boot и потом загрузка Linux не прокатывают.

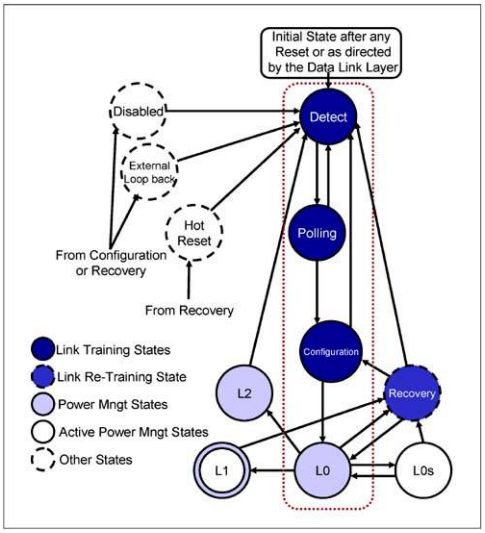
Возможно, это можно как-то обойти (более глубоко сбрасывать трансиверы - PERST недостаточно)

SMARC



LTSSM

link




```
#define LTSSM_DETECT                    0
#define LTSSM_POLLING                   1
#define LTSSM_CONFIG                    2
#define LTSSM_RECOVERY                  3
```

```
#define LTSSM_DISABLED              4
#define LTSSM_HOTRESET              5
#define LTSSM_LOOPBACK              6
#define LTSSM_L0                    7
#define LTSSM_L0s                   8
#define LTSSM_L1                    9
#define LTSSM_L2                    10
```

```
detect.quiet",         /* 0x00 */
detect.active",            /* 0x01 */
polling.active",       /* 0x02 */
polling.compliance",       /* 0x03 */
polling.configuration",        /* 0x04 */
config.linkwidthstart",        /* 0x05 */
config.linkwidthaccept",   /* 0x06 */
config.lanenumwait",       /* 0x07 */
config.lanenumaccept",     /* 0x08 */
config.complete",      /* 0x09 */
config.idle",          /* 0x0A */
recovery.receiverlock",        /* 0x0B */
recovery.equalization",        /* 0x0C */
recovery.speed",       /* 0x0D */
recovery.receiverconfig",  /* 0x0E */
recovery.idle",            /* 0x0F */
L0",               /* 0x10 */
L0s",              /* 0x11 */
L1.entry",         /* 0x12 */
L1.idle",          /* 0x13 */
L2.idle",          /* 0x14 */
L2.transmitwake",      /* 0x15 */
disable",          /* 0x16 */
loopback.entry",       /* 0x17 */
loopback.active",      /* 0x18 */
loopback.exit",            /* 0x19 */
hotreset",         /* 0x1A */
```

Xilinx Xore:

```
00: Detect.Quiet
01: Detect.Active
02: Polling.Active
03: Polling.Compliance
04: Polling.Configuration
05: Configuration.Linkwidth.Start
06: Configuration.Linkwidth.Accept
07: Configuration.Lanenum.Accept
08: Configuration.Lanenum.Wait
09: Configuration.Complete
0A: Configuration.Idle
```

```
0B: Recovery.RcvrLock
0C: Recovery.Speed
0D: Recovery.RcvrCfg
0E: Recovery.Idle
10: L0
11-16: Reserved
17: L1.Entry
18: L1.Idle
19-1A: Reserved
20: Disabled
21: Loopback_Entry_Master
22: Loopback_Active_Master
23: Loopback_Exit_Master
24: Loopback_Entry_Slave
25: Loopback_Active_Slave
26: Loopback_Exit_Slave
27: Hot_Reset
28: Recovery_Equalization_Phase0
29: Recovery_Equalization_Phase1
2a: Recovery_Equalization_Phase2
2b: Recovery_Equalization_Phase3
```