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PCIe

Page	Abbreviation	Description	Tags
ltssm	STSSM	Link Training and Status State Machine	pcie

Docs

https://xilinx.github.io/pcie-debug-kmap/pciedebug/build/html/docs/PCIe_Collaterals/index.html	PCIE DEBUG (GENERAL)
https://support.xilinx.com/s/article/56616?language=en_US	56616 - 7 Series Integrated Block for PCI Express - Link Training Debug Guide
https://support.xilinx.com/s/article/73361?language=en_US	73361 - Xilinx PCI Express Gen3 Link Training Debugging Guide for UltraScale and UltraScale+ Devices
https://support.xilinx.com/s/article/71355?language=en_US	71355 - Vivado ILA Usage Guide for UltraScale FPGA Gen3 Integrated Block for PCI Express
https://support.xilinx.com/s/article/1097525?language=en_US	Debugging PCI Express Link Training Issues with Integrated Debugging Features in the IP
https://github.com/Xilinx/chipscopy/tree/master	ILA, JTAG, DDR, PROGRAM

Connectors

Сторона A (Side A)			Сторона B (Side B)		
A1	PRSNT1#		B1	+12V	

Сторона A (Side A)			Сторона B (Side B)		
A2	+12V		B2	+12V	
A3	+12V		B3	+12V	
A4	GND		B4	GND	
A5	JTAG2		B5	SMBCLK	
A6	JTAG3		B6	SMBDAT	
A7	JTAG4		B7	GND	
A8	JTAG5		B8	+3.3V	
A9	+3.3V		B9	JTAG1	
A10	+3.3V		B10	+3.3Vaux	
A11	PERST#		B11	WAKE#	
A12	GND		B12	CLKREQ#	
A13	REFCLK+		B13	GND	
A14	REFCLK-		B14	PETp0	
A15	GND		B15	PETn0	
A16	PERp0		B16	GND	
A17	PERn0		B17	PRSNT2#	
A18	GND		B18	GND	
A19	RSVD		B19	PETp1	
A20	GND		B20	PETn1	
A21	PERp1		B21	GND	
A22	PERn1		B22	GND	
A23	GND		B23	PETp2	
A24	GND		B24	PETn2	
A25	PERp2		B25	GND	
A26	PERn2		B26	GND	
A27	GND		B27	PETp3	
A28	GND		B28	PETn3	
A29	PERp3		B29	GND	
A30	PERn3		B30	PWRBRK#	
A31	GND		B31	PRSNT2#	
A32	RSVD		B32	GND	
A33	RSVD		B33	PETp4	
A34	GND		B34	PETn4	
A35	PERp4		B35	GND	
A36	PERn4		B36	GND	
A37	GND		B37	PETp5	
A38	GND		B38	PETn5	
A39	PERp5		B39	GND	
A40	PERn5		B40	GND	
A41	GND		B41	PETp6	
A42	GND		B42	PETn6	
A43	PERp6		B43	GND	
A44	PERn6		B44	GND	
A45	GND		B45	PETp7	

Сторона A (Side A)			Сторона B (Side B)		
A46	GND		B46	PETn7	
A47	PERp7		B47	GND	
A48	PERn7		B48	PRSNT2#	
A49	GND		B49	GND	
A50	RSVD		B50	PETp8	
A51	GND		B51	PETn8	
A52	PERp8		B52	GND	
A53	PERn8		B53	GND	
A54	GND		B54	PETp9	
A55	GND		B55	PETn9	
A56	PERp9		B56	GND	
A57	PERn9		B57	GND	
A58	GND		B58	PETp10	
A59	GND		B59	PETn10	
A60	PERp10		B60	GND	
A61	PERn10		B61	GND	
A62	GND		B62	PETp11	
A63	GND		B63	PETn11	
A64	PERp11		B64	GND	
A65	PERn11		B65	GND	
A66	GND		B66	PETp12	
A67	GND		B67	PETn12	
A68	PERp12		B68	GND	
A69	PERn12		B69	GND	
A70	GND		B70	PETp13	
A71	GND		B71	PETn13	
A72	PERp13		B72	GND	
A73	PERn13		B73	GND	
A74	GND		B74	PETp14	
A75	GND		B75	PETn14	
A76	PERp14		B76	GND	
A77	PERn14		B77	GND	
A78	GND		B78	PETp15	
A79	GND		B79	PETn15	
A80	PERp15		B80	GND	
A81	PERn15		B81	PRSNT2#	
A82	GND		B82	RSVD	

Xilinx

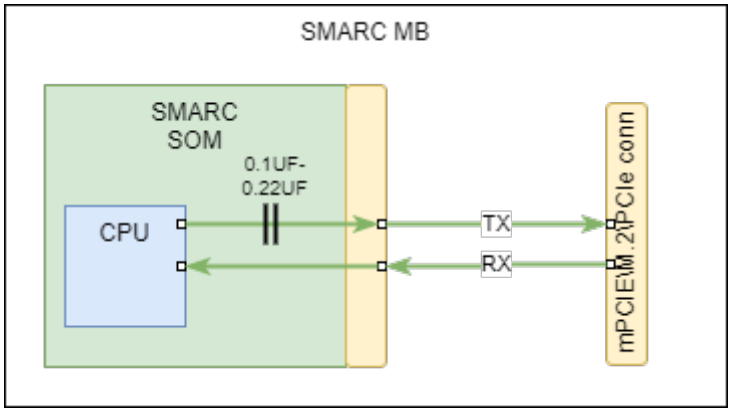
Artix Ultrascale+

PCIe корка стартует нормально только если прошивка быстро загружается из флешки.

Вариант конфигурации через JTAG, а потом ребут компа или пауза в u-boot и потом загрузка Linux не прокатывают.

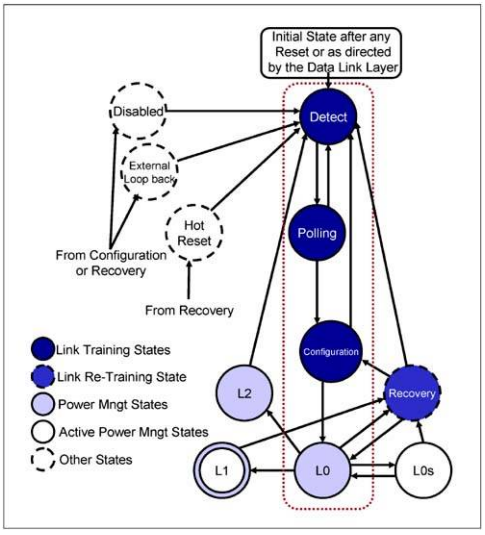
Возможно, это можно как-то обойти (более глубоко сбрасывать трансиверы - PERST недостаточно)

SMARC



LTSSM

link




```
#define LTSSM_DETECT                    0
#define LTSSM_POLLING                   1
#define LTSSM_CONFIG                    2
#define LTSSM_RECOVERY                  3
#define LTSSM_DISABLED                  4
#define LTSSM_HOTRESET                  5
#define LTSSM_LOOPBACK                  6
#define LTSSM_L0                        7
#define LTSSM_L0s                       8
#define LTSSM_L1                        9
```

```
#define LTSSM_L2                    10
```

```
detect.quiet",          /* 0x00 */
detect.active",             /* 0x01 */
polling.active",        /* 0x02 */
polling.compliance",        /* 0x03 */
polling.configuration",         /* 0x04 */
config.linkwidthstart",         /* 0x05 */
config.linkwidthaccept",    /* 0x06 */
config.lanenumwait",        /* 0x07 */
config.lanenumaccept",      /* 0x08 */
config.complete",       /* 0x09 */
config.idle",           /* 0x0A */
recovery.receiverlock",         /* 0x0B */
recovery.equalization",         /* 0x0C */
recovery.speed",        /* 0x0D */
recovery.receiverconfig",   /* 0x0E */
recovery.idle",             /* 0x0F */
L0",                /* 0x10 */
L0s",               /* 0x11 */
L1.entry",          /* 0x12 */
L1.idle",           /* 0x13 */
L2.idle",           /* 0x14 */
L2.transmitwake",       /* 0x15 */
disable",           /* 0x16 */
loopback.entry",        /* 0x17 */
loopback.active",       /* 0x18 */
loopback.exit",             /* 0x19 */
hotreset",          /* 0x1A */
```

Xilinx Xore:

```
00: Detect.Quiet
01: Detect.Active
02: Polling.Active
03: Polling.Compliance
04: Polling.Configuration
05: Configuration.Linkwidth.Start
06: Configuration.Linkwidth.Accept
07: Configuration.Lanenum.Accept
08: Configuration.Lanenum.Wait
09: Configuration.Complete
0A: Configuration.Idle
0B: Recovery.RcvrLock
0C: Recovery.Speed
0D: Recovery.RcvrCfg
0E: Recovery.Idle
10: L0
11-16: Reserved
```

```
17: L1.Entry
18: L1.Idle
19-1A: Reserved
20: Disabled
21: Loopback_Entry_Master
22: Loopback_Active_Master
23: Loopback_Exit_Master
24: Loopback_Entry_Slave
25: Loopback_Active_Slave
26: Loopback_Exit_Slave
27: Hot_Reset
28: Recovery_Equalization_Phase0
29: Recovery_Equalization_Phase1
2a: Recovery_Equalization_Phase2
2b: Recovery_Equalization_Phase3
```