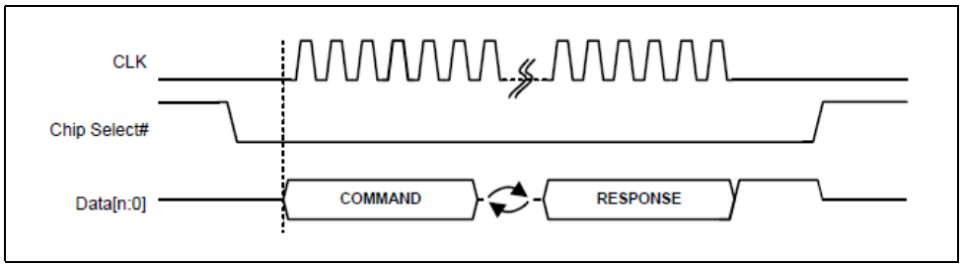
Содержание

eSPI

Enhanced SPI Master Bus Functional Model	https://github.com/akaeba/eSpiMasterBfm
Intel/Altera eSPI to LPC Bridge Core	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_embedded_ip.pdf
Intel eSPI Specification	https://www.intel.com/content/dam/support/us/en/documents/software/chipset-software/327432-004_espi_base_specification_rev1.0_cb.pdf
SmartDV eSPI Slave IIP	https://www.smart-dv.com/iip/espi_slave.html
eSPI protocol	https://www.prodigytechno.com/espi-protocol



IT8883E-I	ITE	eSPI to LPC Bridge	link
ECE1200	Microchip	eSPI to LPC Bridge	link
F85227	fintek	eSPI to LPC Bridge	link

EHL

The eSPI Target has an Alert Mode bit in its General Capabilities and Configuration register, which selects between the discrete and in-band Alert# indications. For a single Initiator – single Target configuration, the default value of this bit (in-band Alert#) works as-is. When two or more targets are present, this bit must be set to 1 by the eSPI Initiator to ensure that Alert# is signaled by discrete pins (one per target).