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SMARC



Разработчик: SGET https://sget.org/

Страничка стандарта: https://sget.org/standards/smarc/

Два типоразмера: 82mm x 50mm и 82mm x 80mm

Разъём - 314pin MXM3.0

Attend	125B-78C00
FOXC	AS0B82*-S43B-*H 4.3 AS0B82*-S55B-*H 5.5 AS0B82*-S78B-*H 7.8 P/N DIM. H AS0B826-S78B-7H
JAE	MM70 Series
Amphenol	MXM-3

Версии стандарта: 1.1, 2.0, 2.1, 2.1.1, 2.2

link	ext	description	manufacturer	version	date	lang
SMARC_DG_V1p0.pdf	pdf	Smart Mobility Architecture Design Guide Version 1.0 July 9, 2013	SGeT	V1.0	2013.07.09	EN

link	ext	description	manufacturer	version	date	lang
SMARC_DG_V2.pdf	pdf	Smart Mobility ARChitecture Design Guide SMARC Design Guide 2.0 March 23, 2017	SGeT	V2.0	2017.03.23	EN
SMARCmodule_DG_V211.pdf	pdf	Smart Mobility ARChitecture Design Guide SMARC Design Guide 2.1.1 April 29, 2021	SGeT	V2.1.1	2021.04.29	EN
SMARCmodule_DG_V22.pdf	pdf	Smart Mobility ARChitecture Design Guide SMARC Design Guide 2.2 2025.06.18	SGeT	V2.2	2025.06.18	EN
SMARC_Hardware_Specification_V1p1.pdf	pdf	Smart Mobility ARChitecture Hardware Specification Version 1.1 May 29, 2014	SGeT	V1.1	2014.05.29	EN
SMARC_Hardware_Specification_V200.pdf	pdf	Smart Mobility ARChitecture Hardware Specification Version 2.0 June 2nd, 2016	SGeT	V2.0	2016.06.02	EN
SMARC_V2_errata1.1.pdf	pdf	Smart Mobility ARChitecture Hardware Specification V2.0 Errata Document	SGeT	v1.1	2015.02.09	EN

link	ext	description	manufacturer	version	date	lang
SMARC_V21-specification.pdf	pdf	Smart Mobility ARChitecture Hardware Specification SMARC 2.1 Specification 2020-03-23	SGeT	V2.1	2020.03.23	EN
SMARC_V211.pdf	pdf	Smart Mobility ARChitecture Hardware Specification SMARC 2.1.1 Specification 2020-05-20	SGeT	V2.1.1	2020.05.20	EN
SMARC_V22_Specification.pdf	pdf	Smart Mobility ARChitecture Hardware Specification SMARC 2.2 Specification 2024.06.12	SGeT	V2.2	2024.06.12	EN

Продукты

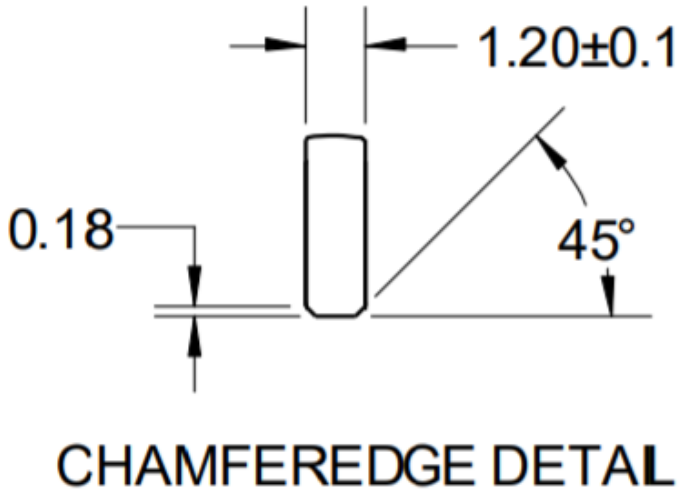
https://sget.org/			
Модули, материнские платы		link	Список ссылок от SGeT
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Модули, материнские платы		link	
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Модули congatec		link	
Материнка congatec	**conga-seval**	link	навороченная
Материнка congatec	**conga-smc1smarc-arm**	link	попроще
https://elvees.ru/			
Модуль elvees на Скиф	**ELV-MC03-SMARC**	https://elvees.ru/	link
https://www.micromax.ru/			

https://sget.org/			
Комп на SMARC модуле на Скиф		link	
https://www.ibase.com.tw/			
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https://portwell.com/			
Модули, материнские платы		link	
https://m.avalue.com.tw/			
Модули, материнские платы		link	
Материнка	**REV-SA03**	link	

img	struct	↓ link	pn	formfactor	manufacturer	cpu	emmc	ram	temprange	dp	hdmi	lvds	ethernet	dsi	csi	usb2	usb3	pcie	can	spi	i2c	smbus	uart	dimension	bios	datasheet_wiki	page_wiki
		adlinktech_lec-el	LEC-EL	SMARC	Adlinktech	Intel® Atom® x6000E Celeron® Pentium® Elkhart Lake	16|32|64 GB	2|4|8 GB LPDDR4x	0...+60|-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp) (NXP PTN3460)	2 (2.5 GBit) (GPY211)	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50	AMI Aptio V	link	page
		advantech-som-2532	SOM-2532	SMARC	Advantech	Intel® Atom® x6000E Celeron® Pentium® Elkhart Lake	64 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2 (Marvell 88E1512)	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50	AMI Aptio V	link	page
		congatec_conga-sa5	conga-SA5	SMARC	Congatec	Intel Atom E3900	32 GB	8 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2 (i210, i211)	1 (or edp|lvds 2ch)	2 (x4, x2)	6	2	up to 4 gen2	2	2	2		4 (2 full)	82x50	AMI Aptio® V UEFI 2.x firmware, 8 MB serial SPI	link	page
		congatec_conga-sa7	conga-SA7	SMARC	Congatec	Intel Atom x6000E	128 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	up to 4	1 (or edp|lvds 2ch)		6	2	up to 4 gen3	2	2	2		4 (2 full)	82x50	AMI Aptio 32 MB serial SPI	link	page
		data_modul_edm-smx-el	eDM-SMX-EL	SMARC	Data Modul	Intel® Atom® x6000E Celeron® Pentium® Elkhart Lake	64 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50	AMI Aptio V	link	page
		kontron_smarc-sxel_e2	SMARC-sXEL E2	SMARC	Kontron	Intel® Atom® x6000E Celeron® Pentium® Elkhart Lake	64 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50	AMI Aptio V	link	page
		seco_som-smarc-ehl	SOM-SMARC-EHL	SMARC	SECO	Intel® Atom® x6000E Celeron® Pentium® Elkhart Lake	64 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50	AMI Aptio V	link	page
		tq-embedded_tqmxe39s	TQMxE39S	SMARC	TQ-Embedded	Intel Atom® x5|x7 E3900 series ("Apollo Lake-I") Pentium® N4200 and Celeron® N3350 processors	64 GB	8 GB LPDDR4	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	1 (i210)		2	4 (1 OTG)	2	4 gen 2 (1x4, 2x2, 4x1)		1	1	1	4	82x50		link	page
		tq-embedded_tqmxe40s	TQMxE40S	SMARC	TQ-Embedded	Intel Atom® x6000 series Elkhart Lake	256 GB	16 GB LPDDR4x	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2	1 (or edp|lvds 2ch)		4	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi	1	1	4 (2 full)	82x50		link	page
		tq-embedded_tqmxe41s	TQMxE41S	SMARC	TQ-Embedded	Intel® Atom® x7000E Celeron® Pentium® Alder Lake-N	256 GB	16 GB LPDDR5	-40...+85 °C	2 (or 1 hdmi)	1 (or dp)	1 2ch(or dsi|edp)	2 (2.5Gb Intel i226)	1 (or edp|lvds 2ch)		6	2	4 gen 3 (1x4, 2x2, 4x1)	2	1 + 1 espi			4 (2 full)	82x50		link	page

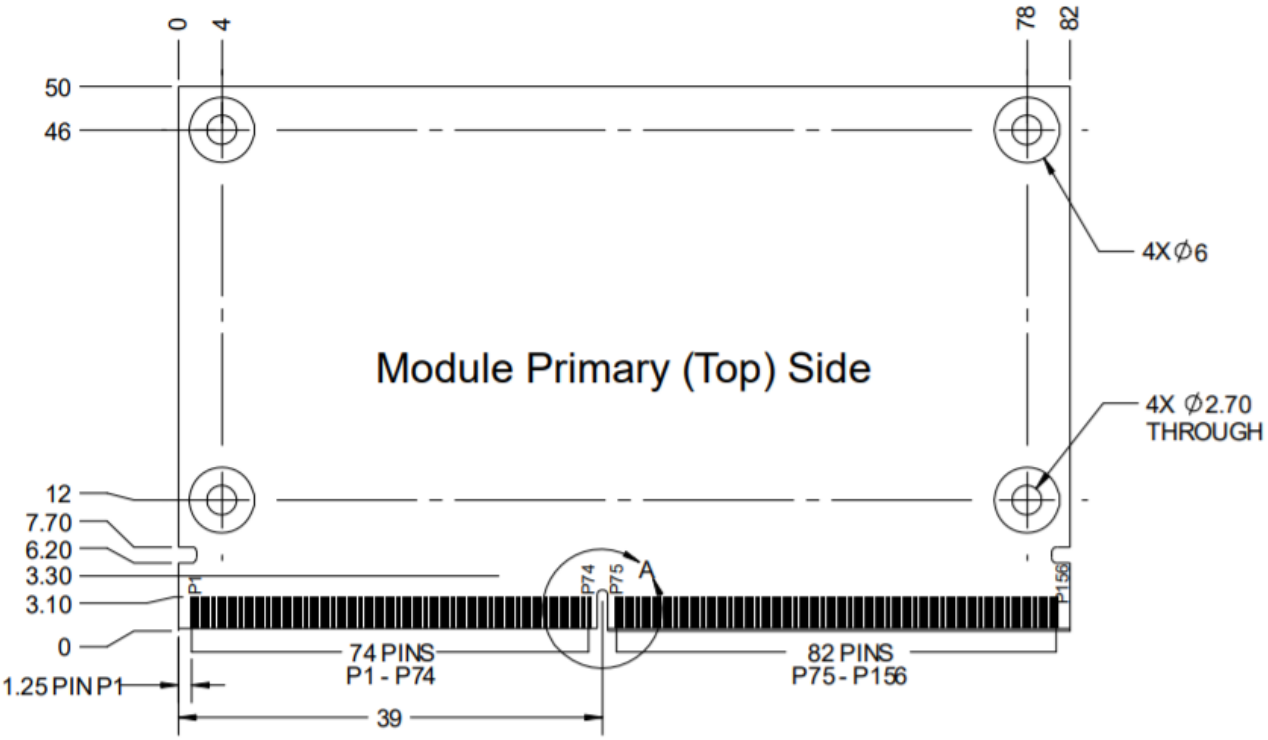
Размеры

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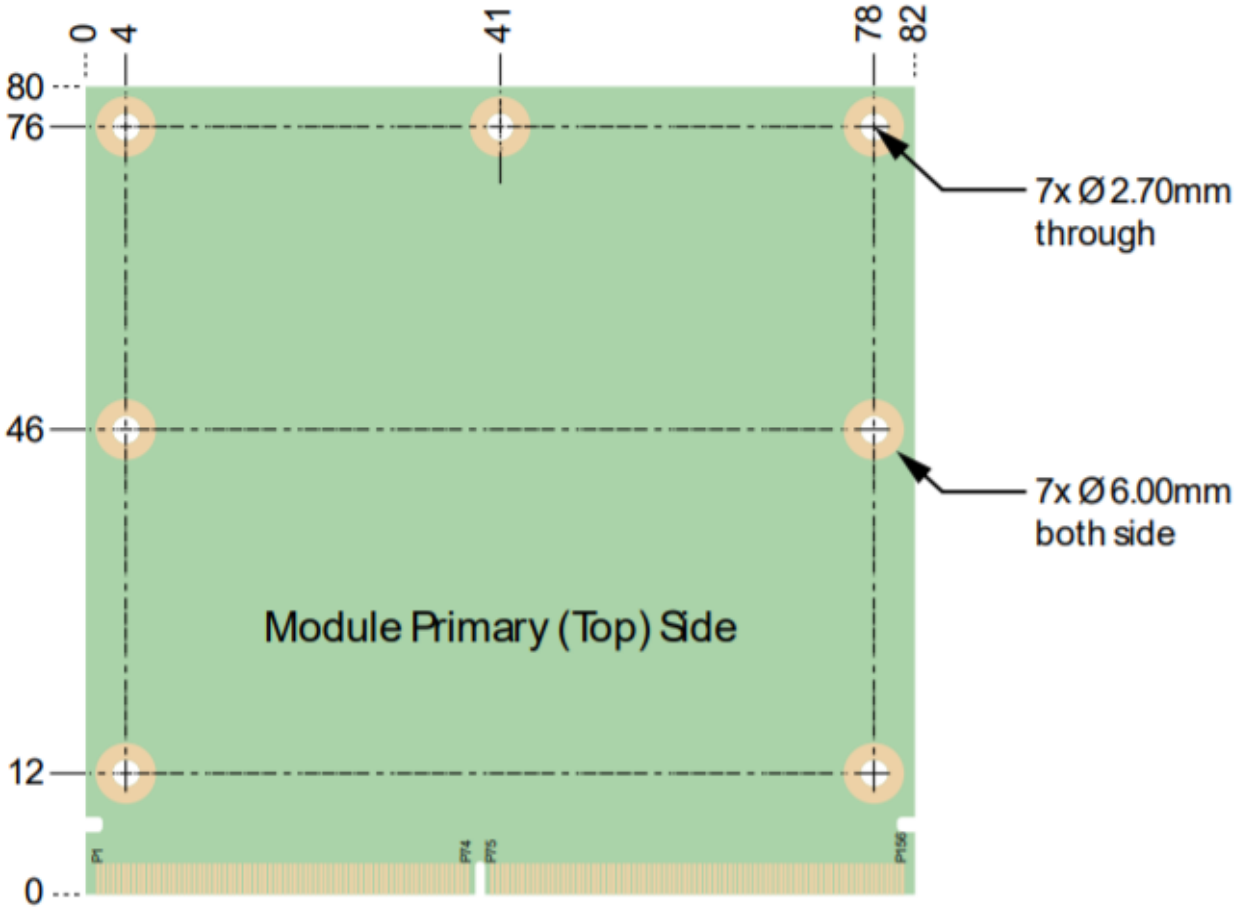




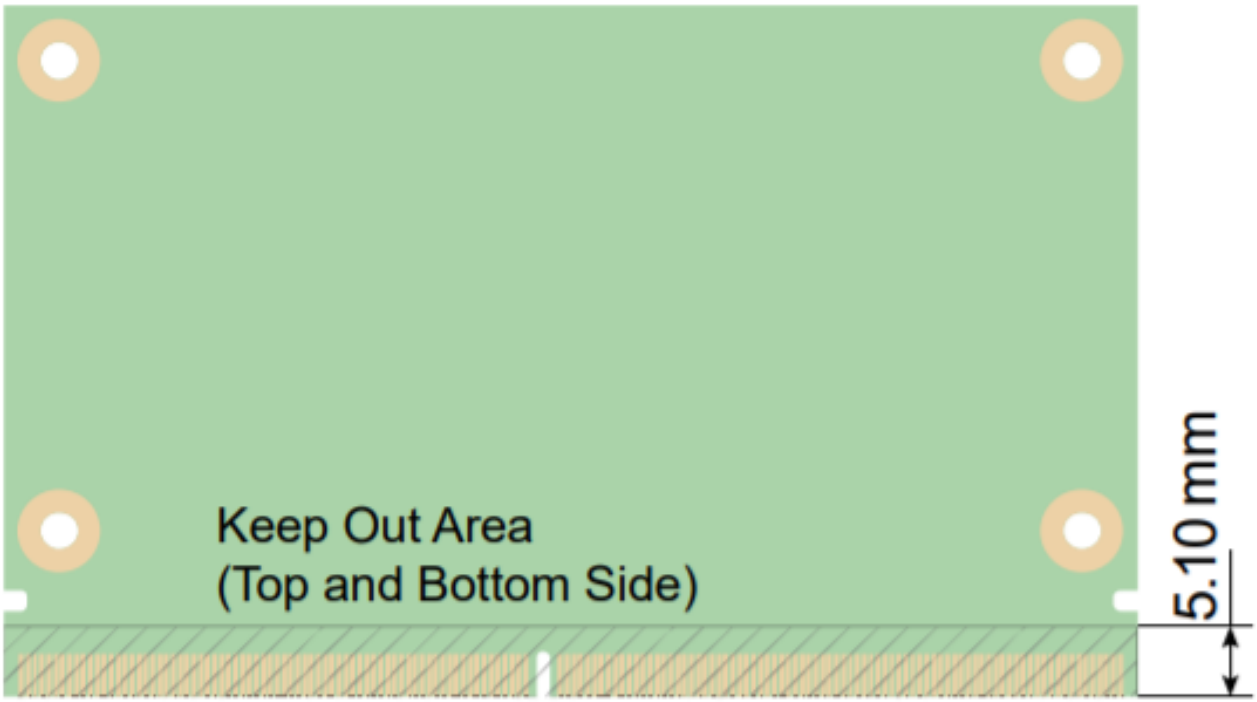
Модуль 82x50мм:



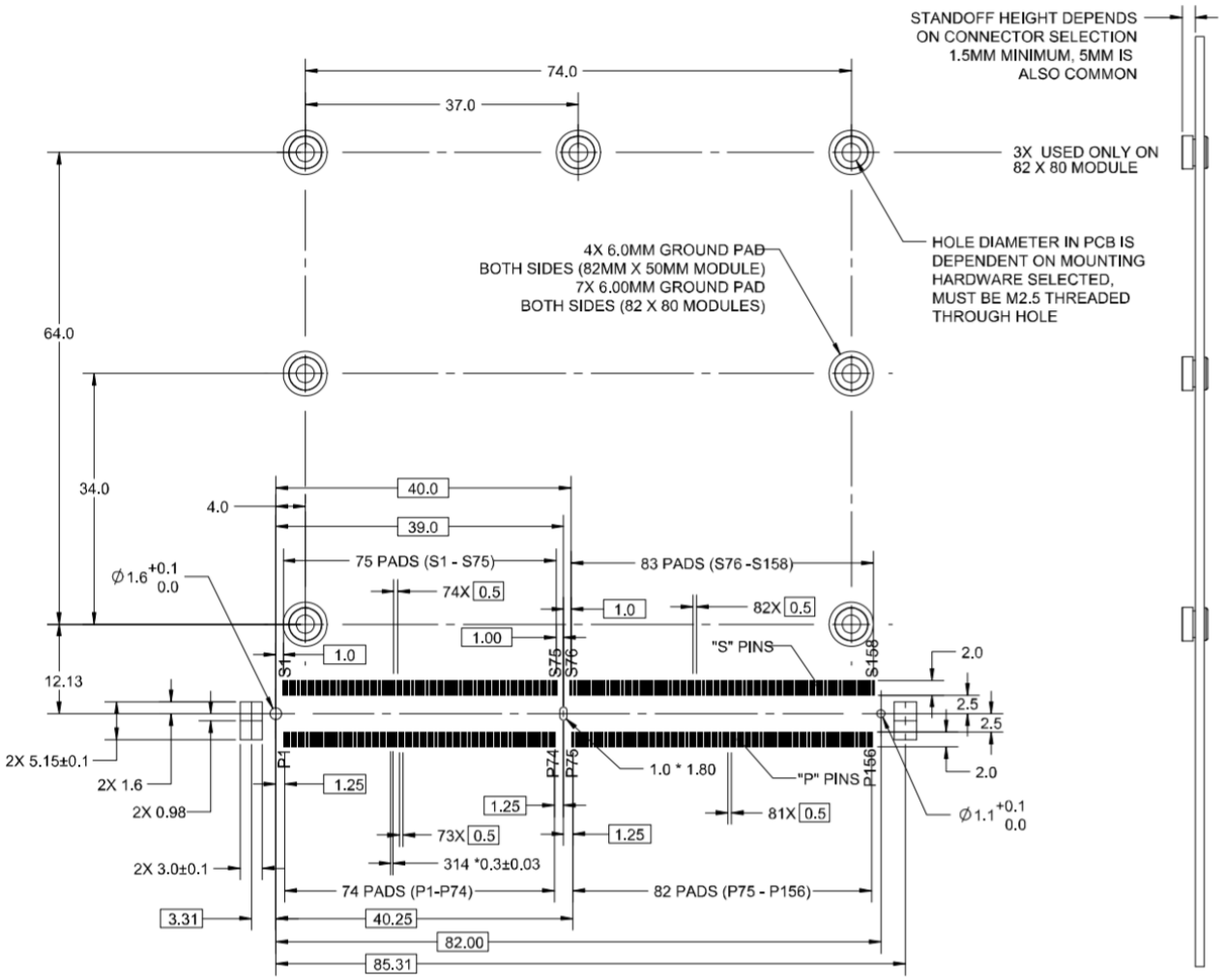
Модуль 82x80мм:



KeepOut area:



Ответная часть на материнской плате:



Power

Module input voltage range: **VDD_IN** 3.0V to 5.25V

RTC power rail: **VDD_RTC**: 2.0V to 3.25V

Power sequence:

Power up with sleep power domain and PWR_BTN#
Power up sequence with sleep power domain without PWR_BTN#
Power up sequence without sleep power domain and with PWR_BTN#
Power up sequence without sleep power domain and without PWR_BTN#

MODULE AND CARRIER SERIAL EEPROMS

- SMARC Modules **should** include an I2C serial EEPROM on the Module I2C_GP bus.
- SMARC Carriers **may** include an I2C serial EEPROM on the I2C_PM bus, in the Module power domain.

pcb routing

Table 21 High-Speed Differential Trace Parameters

Interface	Max Symbol Rate (approximate)	Sym Width (ps)	Zo Diff (ohms)	Zo SE (ohms)	Max Length (mils)	Pair Match (mils)	Group Match (mils)	TX / RX Match (mils)
PCIe	8 Gbps (Gen 3) 5 Gbps (Gen 2) 2.5 Gbps (Gen 1)	125 200 500	85 (+-15%)	50	5,000 10,000 12,000	< 5	N/A	< 2000
SATA	6 Gbps (Gen 3) 3 Gbps (Gen 2) 1.5 Gbps (Gen 1)	167 333 667	85 (+-20%)	50 (+-15%)	3,000 6,000 8,000	< 5	N/A	< 2000
HDMI	3.4 Gbps (HDMI 1.3) 1.6 Gbps (HDMI 1.2) 1.6 Gbps (HDMI 1.1) 1.6 Gbps (HDMI 1.0)	294 625 625 625	90	45	5,000	< 10	< 830	N/A
CSI	1 Gbps (CSI-2) 208 Mbps (CSI)	1000 4808	90	45	9,000	< 100	< 100	N/A
LVDS	770 Mbps (24b 110 MHz) 280 Mbps (24b 40 MHz)	1299 3571	100 (+-20%)	50	6,750	< 20	< 20	N/A
USB 2.0	480 Mbps (HS) 12 Mbps (FS)	2083 23333	90	45	10,000	< 100	N/A	N/A
USB 3.0	5 Gbps	N/A	85 (+-10%)	50 (+-15%)	4,500	< 5	N/A	N/A
GBE	250 Mbps	N/A	100	50	4,000	< 5	< 30	N/A
DP++	8.1 Gbps	N/A	85 (+-10%)	50 (+-10%)	3,200	< 5	< 1000	N/A

Table 23 High-Speed Differential Trace Parameters (Example)

Interface	Max Symbol Rate (approximate)	Sym Width (ps)	Zo Diff (ohms)	Zo SE (ohms)	Max Length [1] (mils)	Pair Match (mils)	Group Match (mils)	TX / RX Match (mils)
PCIe Device Down	16 Gbps (Gen 4) [2]	62.5	85	50	5,900	< 2.5	N/A	< 1000
	8 Gbps (Gen 3)	125	(+-15%)	(+-10%)	4,400			
	5 Gbps (Gen 2)	200			6,400			
	2.5 Gbps (Gen 1)	500			9,400			
PCIe Addin Card	16 Gbps (Gen 4) [2]	62.5	85	50	4,000	< 2.5	N/A	< 1000
	8 Gbps (Gen 3)	125	(+-15%)	(+-10%)	3,600			
	5 Gbps (Gen 2)	200			4,500			
	2.5 Gbps (Gen 1)	500			8,500			
SATA	6 Gbps (Gen 3)	167	85	50	3,200	< 2.5	N/A	< 1000
	3 Gbps (Gen 2)	333	(+-20%)	(+-15%)	3,700			
	1.5 Gbps (Gen 1)	667			3,800			
HDMI	6 Gbps (HDMI 2.0) [3]	167	90	45	9,000	< 5	< 415	N/A
	3.4 Gbps (HDMI 1.3-1.4) [4]	294			5,100			
	1.6 Gbps (HDMI 1.0-1.2) [5]	625			2,700 [5]			
DP++ / DP / eDP	8.1 Gbps (DP 1.3-1.4) [2]	123	85	50	1,400	< 2.5	< 500	N/A
	5.4 Gbps (DP 1.2)	185	(+-10%)	(+-10%)	2,000			
LVDS	770 Mbps (24b 110 MHz)	1299	100	50	6,700	< 10	< 10	N/A
	280 Mbps (24b 40 MHz)	3571	(+-20%)		6,700			
MIPI-DSI	2.5 Gbps (DSI 1.2) D-Phy	400	90	45	3,500	< 2.5	< 20	N/A
MIPI-CSI	2.5 Gbps (CSI-2) D-Phy	400	90	45	3,700	< 2.5	< 20	N/A
USB 3.2 gen2	10 Gbps (SuperSpeed lines) [2]	100	85 (+-10%)	50 (+-15%)	500 [6]	< 2.5	N/A	N/A
USB 3.2 gen1	5 Gbps (SuperSpeed lines)	200	85 (+-10%)	50 (+-15%)	4,000	< 2.5	N/A	N/A
USB 2.0	480 Mbps (HS)	2083	90	45	8,000	< 50	N/A	N/A
	12 Mbps (FS)	23333			8,000			
2.5 GBE	625 Mbps	N/A	100	50	3,000	< 2.5	< 15	N/A
1 GBE	250 Mbps	N/A	100	50	7,200	< 2.5	< 15	N/A

Reference Plane: GND is preferred

Clearance to other traces: 20 mil or more

Max Vias: 2 (or less preferred)

Разъём

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P001	P1	SMB_ALERT#	MANAGEMENT	I OD CMOS	1V8...5V	PU 2K2	SMBus Alert# (Interrupt) Signal	Standby/Sleep	
P002	P2	GND	PWR GND						
P003	P3	CSI1_CK+	CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P004	P4	CSI1_CK-	CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	
P005	P5	GBE1_SDP	GBE1	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P006	P6	GBE0_SDP	GBE0	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P007	P7	CSI1_RX0+	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P008	P8	CSI1_RX0-	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P009	P9	GND	PWR GND						
P010	P10	CSI1_RX1+	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P011	P11	CSI1_RX1-	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P012	P12	GND	PWR GND						
P013	P13	CSI1_RX2+	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P014	P14	CSI1_RX2-	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P015	P15	GND	PWR GND						
P016	P16	CSI1_RX3+	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P017	P17	CSI1_RX3-	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P018	P18	GND	PWR GND						
P019	P19	GBE0_MDI3-	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P020	P20	GBE0_MDI3+	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P021	P21	GBE0_LINK100#	GBE0	O OD CMOS	3V3		Link Speed Indication LED for GBE0 100Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P022	P22	GBE0_LINK1000#	GBE0	O OD CMOS	3V3		Link Speed Indication LED for GBE0 1000Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
P023	P23	GBE0_MDI2-	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P024	P24	GBE0_MDI2+	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P025	P25	GBE0_LINK_ACT#	GBE0	O OD CMOS	3V3		Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	Shall be able to sink 24mA or more Carrier LED current.
P026	P26	GBE0_MDI1-	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P027	P27	GBE0_MDI1+	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P028	P28	GBE0_CTREF	GBE0	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
P029	P29	GBE0_MDI0-	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P030	P30	GBE0_MDI0+	GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P031	P31	SPI0_CS1#	SPI0	O CMOS	1V8		SPI0 Master Chip Select 1	Standby	
P032	P32	GND	PWR GND						
P033	P33	SDIO_WP	SDIO	I OD CMOS	1V8 or 3V3	PU 10k	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	Runtime	
P034	P34	SDIO_CMD	SDIO	I/O CMOS	1V8 or 3V3		SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	Runtime	
P035	P35	SDIO_CD#	SDIO	I OD CMOS	1V8 or 3V3	PU 10k	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P036	P36	SDIO_CK	SDIO	O CMOS	1V8 or 3V3		SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	Runtime	SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
P037	P37	SDIO_PWR_EN	SDIO	O CMOS	3V3		SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	Runtime	Should be driven low in Standby Mode by the Module
P038	P38	GND	PWR GND						
P039	P39	SDIO_D0	SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P040	P40	SDIO_D1	SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P041	P41	SDIO_D2	SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P042	P42	SDIO_D3	SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P043	P43	SPI0_CS0#	SPI0	O CMOS	1V8		SPI0 Master Chip Select 0	Standby	This signal can be used to select Carrier SPI as boot device
P044	P44	SPI0_CK	SPI0	O CMOS	1V8		SPI0 Clock	Standby	
P045	P45	SPI0_DIN	SPI0	I CMOS	1V8		SPI0 Master input / Slave output	Standby	also referred to as MISO
P046	P46	SPI0_DO	SPI0	O CMOS	1V8		SPI0 Master output / Slave input	Standby	also referred to as MOSI
P047	P47	GND	PWR GND						
P048	P48	SATA_TX+	SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P049	P49	SATA_TX-	SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P050	P50	GND	PWR GND						
P051	P51	SATA_RX+	SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P052	P52	SATA_RX-	SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P053	P53	GND	PWR GND						
P054	P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	SPI1	O CMOS	1V8		SPI1 Master Chip Select 0	Standby	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P054	P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	QSPI	O CMOS	1V8		QSPI Master Chip Select 0	Standby	
P054	P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	eSPI	O CMOS	1V8		ESPI1 Master Chip Select 0	Standby	
P055	P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	SPI1	O CMOS	1V8		SPI1 Master Chip Select 1	Standby	
P055	P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	QSPI	O CMOS	1V8		QSPI Master Chip Select 1	Standby	
P055	P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	eSPI	O CMOS	1V8		ESPI1 Master Chip Select 1	Standby	
P056	P56	ESPI_CK / SPI1_CK / QSPI_CK	SPI1	O CMOS	1V8		SPI1 Clock	Standby	
P056	P56	ESPI_CK / SPI1_CK / QSPI_CK	QSPI	O CMOS	1V8		QSPI Clock	Standby	
P056	P56	ESPI_CK / SPI1_CK / QSPI_CK	eSPI	O CMOS	1V8		ESPI Master Clock Output	Standby	
P057	P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	SPI1	I CMOS	1V8		SPI1 Master input / Slave output	Standby	also referred to as MISO
P057	P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
P057	P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	eSPI	I/O CMOS	1V8		ESPI Master Data Input / Output	Standby	
P058	P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	SPI1	O CMOS	1V8		SPI1 Master output / Slave input	Standby	also referred to as MOSI
P058	P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
P058	P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	eSPI	I/O CMOS	1V8		ESPI Master Data Input / Output	Standby	In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO)
P059	P59	GND	PWR GND						
P060	P60	USB0+	USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P061	P61	USB0-	USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P062	P62	USB0_EN_OC#	USB0	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 0	Standby	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate overcurrent situation.

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P063	P63	USB0_VBUS_DET	USB0	I USB VBUS 5V	USB VBUS 5V		USB Port 0 Host Power Detection	Standby	
P064	P64	USB0_OTG_ID	USB0				Input Pin to Announce OTG Device Insertion on USB 2.0 Port	Standby	
P065	P65	USB1+	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P066	P66	USB1-	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P067	P67	USB1_EN_OC#	USB1	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 1	Standby	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P068	P68	GND	PWR GND						
P069	P69	USB2+	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P070	P70	USB2-	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P071	P71	USB2_EN_OC#	USB2	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 2	Standby	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P072	P72	RSVD							
P073	P73	RSVD							
P074	P74	USB3_EN_OC#	USB3	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 3	Standby	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P075	P75	PCIE_A_RST#	PCIEA	O CMOS	3V3		PCIe Port A reset output	Runtime	
P076	P76	USB4_EN_OC#	USB4	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 4	Standby	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate overcurrent situation.

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P077	P77	PCIE_B_CKREQ#	PCIEB	IO OD CMOS	3V3	PU >10K	PCIe Port B clock request	Runtime	
P078	P78	PCIE_A_CKREQ#	PCIEA	IO OD CMOS	3V3	PU >10K	PCIe Port A clock request	Runtime	
P079	P79	GND	PWR GND						
P080	P80	PCIE_C_REFCK+	PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P081	P81	PCIE_C_REFCK-	PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P082	P82	GND	PWR GND						
P083	P83	PCIE_A_REFCK+	PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	
P084	P84	PCIE_A_REFCK-	PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	
P085	P85	GND	PWR GND						
P086	P86	PCIE_A_RX+	PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P087	P87	PCIE_A_RX-	PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P088	P88	GND	PWR GND						
P089	P89	PCIE_A_TX+	PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P090	P90	PCIE_A_TX-	PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P091	P91	GND	PWR GND						
P092	P92	HDMI_D2+ / DP1_LANE0+	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P092	P92	HDMI_D2+ / DP1_LANE0+	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P093	P93	HDMI_D2- / DP1_LANE0-	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P093	P93	HDMI_D2- / DP1_LANE0-	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P094	P94	GND	PWR GND						
P095	P95	HDMI_D1+ / DP1_LANE1+	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P095	P95	HDMI_D1+ / DP1_LANE1+	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P096	P96	HDMI_D1- / DP1_LANE1-	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P096	P96	HDMI_D1- / DP1_LANE1-	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P097	P97	GND	PWR GND						
P098	P98	HDMI_D0+ / DP1_LANE2+	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P098	P98	HDMI_D0+ / DP1_LANE2+	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P099	P99	HDMI_D0- / DP1_LANE2-	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P099	P99	HDMI_D0- / DP1_LANE2-	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P100	P100	GND	PWR GND						
P101	P101	HDMI_CK+ / DP1_LANE3+	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P101	P101	HDMI_CK+ / DP1_LANE3+	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P102	P102	HDMI_CK- / DP1_LANE3-	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P102	P102	HDMI_CK- / DP1_LANE3-	DP1++	O DP			Secondary DP Port Differential Pair Data Lines	Runtime	
P103	P103	GND	PWR GND						
P104	P104	HDMI_HPD / DP1_HPD	HDMI	I CMOS	1V8	PD 1M	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	Runtime	
P104	P104	HDMI_HPD / DP1_HPD	DP1++	I CMOS	1V8	PD 1M	DP Hot Plug Detect Input	Runtime	
P105	P105	HDMI_CTRL_CK / DP1_AUX+	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_CLK Line Dedicated to HDMI	Runtime	
P105	P105	HDMI_CTRL_CK / DP1_AUX+	DP1++	I/O DP	3V3	PD 100K	Secondary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC Coupled on module (DC coupled if HDMI)
P106	P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_DAT Line Dedicated to HDMI	Runtime	
P106	P106	HDMI_CTRL_DAT / DP1_AUX-	DP1++	I/O DP	3V3	PU 100K	Secondary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC Coupled on module (DC coupled if HDMI)
P107	P107	DP1_AUX_SEL	DP1++_HDMI	I CMOS	1V8	PD 1M	Strapping Signal to Enable Either HDMI or DP Output	Runtime	0 - DP 1 - HDMI
P108	P108	GPIO0 / CAM0_PWR#	CSI0	O CMOS	1V8		Camera 0 Power Enable, active low output.	Runtime	Shared with GPIO0
P108	P108	GPIO0 / CAM0_PWR#	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 0 Preferred Output	Runtime	Shared with CAM0_PWR#
P109	P109	GPIO1 / CAM1_PWR#	CSI1	O CMOS	1V8		Camera 1 Power Enable, active low output.	Runtime	Shared with GPIO1
P109	P109	GPIO1 / CAM1_PWR#	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 1 Preferred Output	Runtime	Shared with CAM1_PWR#
P110	P110	GPIO2 / CAM0_RST#	CSI0	O CMOS	1V8		Camera 0 reset, active low output	Runtime	Shared with GPIO2
P110	P110	GPIO2 / CAM0_RST#	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 2 Preferred Output	Runtime	Shared with CAM0_RST#

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P111	P111	GPIO3 / CAM1_RST#	CSI1	O CMOS	1V8		Camera 0 reset, active low output	Runtime	Shared with GPIO3
P111	P111	GPIO3 / CAM1_RST#	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 3 Preferred Output	Runtime	Shared with CAM1_RST#
P112	P112	GPIO4 / HDA_RST#	HDA	O CMOS	1V8 / 1V5		High Definition Audio Reset Output to Codec, low active.	Runtime	
P112	P112	GPIO4 / HDA_RST#	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 4 Preferred Output	Runtime	Shared with HDA_RST#
P113	P113	GPIO5 / PWM_OUT	FAN	O CMOS	1V8	PU 470K	Fan Speed Control	Runtime	
P113	P113	GPIO5 / PWM_OUT	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 5 Preferred Output	Runtime	Shared with PWM_OUT
P114	P114	GPIO6 / TACHIN	FAN	O CMOS	1V8	PU 470K	Fan Tachometer Input	Runtime	
P114	P114	GPIO6 / TACHIN	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 6 Preferred Output	Runtime	Shared with TACHIN
P115	P115	GPIO7	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 7 Preferred Output	Runtime	
P116	P116	GPIO8	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 8 Preferred Output	Runtime	
P117	P117	GPIO9	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 9 Preferred Output	Runtime	
P118	P118	GPIO10	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 10 Preferred Output	Runtime	
P119	P119	GPIO11	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 11 Preferred Output	Runtime	
P120	P120	GND	PWR GND						
P121	P121	I2C_PM_CK	MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus CLK	Standby/Sleep	
P122	P122	I2C_PM_DAT	MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus DATA	Standby/Sleep	
P123	P123	BOOT_SEL0#	BOOT	I OD CMOS	1V8	PU 10K	Input straps determine the Module boot device.	Standby	
P124	P124	BOOT_SEL1#	BOOT	I OD CMOS	1V8	PU 10K	Input straps determine the Module boot device.	Standby	
P125	P125	BOOT_SEL2#	BOOT	I OD CMOS	1V8	PU 10K	Input straps determine the Module boot device.	Standby	
P126	P126	RESET_OUT#	MANAGEMENT	O CMOS	1V8		General purpose reset output to Carrier Board.	Standby	
P127	P127	RESET_IN#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal Shall be level triggered during bootup to allow to stop booting of the module. After bootup it May act as an edge triggered signal.	Standby	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
P128	P128	POWER_BTN#	MANAGEMENT	I OD CMOS	1V8...5V	PU 10K	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Sleep	
P129	P129	SER0_TX	SER0	O CMOS	1V8		Asynchronous Serial Data Output Port 0	Runtime	
P130	P130	SER0_RX	SER0	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 0	Runtime	
P131	P131	SER0_RTS#	SER0	O CMOS	1V8		Request to Send Handshake Line for Port 0	Runtime	
P132	P132	SER0_CTS#	SER0	I CMOS	1V8	PU 100K	Clear to Send Handshake Line for Port 0	Runtime	
P133	P133	GND	PWR GND						
P134	P134	SER1_TX	SER1	O CMOS	1V8		Asynchronous Serial Data Output Port 1	Runtime	
P135	P135	SER1_RX	SER1	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 1	Runtime	
P136	P136	SER2_TX	SER2	O CMOS	1V8		Asynchronous Serial Data Output Port 2	Runtime	
P137	P137	SER2_RX	SER2	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 2	Runtime	
P138	P138	SER2_RTS#	SER2	O CMOS	1V8		Request to Send Handshake Line for Port 2	Runtime	
P139	P139	SER2_CTS#	SER2	I CMOS	1V8	PU 100K	Clear to Send Handshake Line for Port 2	Runtime	
P140	P140	SER3_TX	SER3	O CMOS	1V8		Asynchronous Serial Data Output Port 3	Runtime	
P141	P141	SER3_RX	SER3	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 3	Runtime	
P142	P142	GND	PWR GND						
P143	P143	CAN0_TX	CAN0	O CMOS	1V8		CAN Port 0 Transmit Output	Runtime	
P144	P144	CAN0_RX	CAN0	I CMOS	1V8		CAN Port 0 Receive Input	Runtime	
P145	P145	CAN1_TX	CAN1	O CMOS	1V8		CAN Port 1 Transmit Output	Runtime	
P146	P146	CAN1_RX	CAN1	I CMOS	1V8		CAN Port1 Receive Input	Runtime	
P147	P147	VDD_IN	PWR		3V...5.25V				
P148	P148	VDD_IN	PWR		3V...5.25V				
P149	P149	VDD_IN	PWR		3V...5.25V				
P150	P150	VDD_IN	PWR		3V...5.25V				
P151	P151	VDD_IN	PWR		3V...5.25V				
P152	P152	VDD_IN	PWR		3V...5.25V				
P153	P153	VDD_IN	PWR		3V...5.25V				
P154	P154	VDD_IN	PWR		3V...5.25V				
P155	P155	VDD_IN	PWR		3V...5.25V				
P156	P156	VDD_IN	PWR		3V...5.25V				
S001	S1	CSI1_TX+ / I2C_CAM1_CK	CSI1	I/O OD CMOS	1V8	PU 2k2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S001	S1	CSI1_TX+ / I2C_CAM1_CK	CSI1	O M-PHY			serial camera differential data lane	Runtime	CSI3.0
S002	S2	CSI1_TX- / I2C_CAM1_DAT	CSI1	I/O OD CMOS	1V8	PU 2k2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S002	S2	CSI1_TX- / I2C_CAM1_DAT	CSI1	O M-PHY			serial camera differential data lane	Runtime	CSI3.0
S003	S3	GND	PWR GND						
S004	S4	RSVD							
S005	S5	CSI0_TX+ / I2C_CAM0_CK	CSI0	I/O OD CMOS	1V8	PU 2k2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0
S005	S5	CSI0_TX+ / I2C_CAM0_CK	CSI0	O M-PHY			serial camera differential data lane	Runtime	CSI3.0
S006	S6	CAM_MCK	CSI	O CMOS	1V8		Master clock output	Runtime	
S007	S7	CSI0_TX- / I2C_CAM0_DAT	CSI0	I/O OD CMOS	1V8	PU 2k2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S007	S7	CSI0_TX- / I2C_CAM0_DAT	CSI0	O M-PHY			serial camera differential data lane	Runtime	CSI3.0
S008	S8	CSI0_CK+	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S009	S9	CSI0_CK-	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S010	S10	GND	PWR GND						
S011	S11	CSI0_RX0+	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S012	S12	CSI0_RX0-	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S013	S13	GND	PWR GND						
S014	S14	CSI0_RX1+	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S015	S15	CSI0_RX1-	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S016	S16	GND	PWR GND						
S017	S17	GBE1_MDI0+	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S018	S18	GBE1_MDI0-	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S019	S19	GBE1_LINK100#	GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 100Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
S020	S20	GBE1_MDI1+	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S021	S21	GBE1_MDI1-	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S022	S22	GBE1_LINK1000#	GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 1000Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
S023	S23	GBE1_MDI2+	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S024	S24	GBE1_MDI2-	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S025	S25	GND	PWR GND						
S026	S26	GBE1_MDI3+	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S027	S27	GBE1_MDI3-	GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S028	S28	GBE1_CTREF	GBE1	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
S029	S29	PCIE_D_TX+ / SERDES_0_TX+	PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S029	S29	PCIE_D_TX+ / SERDES_0_TX+	SERDES0	O PCIE			Differential SERDES 0 Transmit Data Pair	Runtime	Series AC coupled on Module
S030	S30	PCIE_D_TX- / SERDES_0_TX-	PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S030	S30	PCIE_D_TX- / SERDES_0_TX-	SERDES0	O PCIE			Differential SERDES 0 Transmit Data Pair	Runtime	Series AC coupled on Module
S031	S31	GBE1_LINK_ACT#	GBE1	O OD CMOS	3V3		Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	Shall be able to sink 24mA or more Carrier LED current.
S032	S32	PCIE_D_RX+ / SERDES_0_RX+	PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S032	S32	PCIE_D_RX+ / SERDES_0_RX+	SERDES0	I PCIE			Differential SERDES 0 Receive Data Pair	Runtime	
S033	S33	PCIE_D_RX- / SERDES_0_RX-	PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S033	S33	PCIE_D_RX- / SERDES_0_RX-	SERDES0	I PCIE			Differential SERDES 0 Receive Data Pair	Runtime	
S034	S34	GND	PWR GND						
S035	S35	USB4+	USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S036	S36	USB4-	USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S037	S37	USB3_VBUS_DET	USB3	I USB VBUS 5V	USB VBUS 5V		USB Port 3 Host Power Detection	Standby	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S038	S38	AUDIO_MCK	I2S	O CMOS	1V8		Master Clock Output to I2S Codec(s)	Runtime	
S039	S39	I2S0_LRCK	I2S0	I/O CMOS	1V8		I2S0 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S040	S40	I2S0_SDOUT	I2S0	O CMOS	1V8		I2S0 Digital Audio Output	Runtime	
S041	S41	I2S0_SDIN	I2S0	I CMOS	1V8		I2S0 Digital Audio Input	Runtime	
S042	S42	I2S0_CK	I2S0	I/O CMOS	1V8		I2S0 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S043	S43	ESPI_ALERT0#	eSPI	I OD CMOS	1V8	PU 4K7	ESPI ALERT	Standby	
S044	S44	ESPI_ALERT1#	eSPI	I OD CMOS	1V8	PU 4K7	ESPI ALERT	Standby	
S045	S45	MDIO_CLK	SERDES	O CMOS	1V8		MDIO Signals to Configure Possible PHYs		
S046	S46	MDIO_DAT	SERDES	I/O OD CMOS	1V8	PU 1K5	MDIO Signals to Configure Possible PHYs		
S047	S47	GND	PWR GND						
S048	S48	I2C_GP_CK	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Clock Signal	Runtime	
S049	S49	I2C_GP_DAT	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Data Signal	Runtime	
S050	S50	HDA_SYNC / I2S2_LRCK	I2S2	I/O CMOS	1V8		I2S2 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S050	S50	HDA_SYNC / I2S2_LRCK	HDA	I/O CMOS	1V8/1V5		High Definition Audio Sample synchronization clock to codec	Runtime	
S051	S51	HDA_SDO / I2S2_SDOUT	I2S0	O CMOS	1V8		I2S2 Digital Audio Output	Runtime	
S051	S51	HDA_SDO / I2S2_SDOUT	HDA	O CMOS	1V8/1V5		High Definition Audio data out to codec	Runtime	
S052	S52	HDA_SDI / I2S2_SDIN	I2S0	I CMOS	1V8		I2S2 Digital Audio Input	Runtime	
S052	S52	HDA_SDI / I2S2_SDIN	HDA	I/O CMOS	1V8/1V5		High Definition Audio data in from codec	Runtime	
S053	S53	HDA_CK / I2S2_CK	I2S0	I/O CMOS	1V8		I2S2 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S053	S53	HDA_CK / I2S2_CK	HDA	O CMOS	1V8/1V5		High Definition Audio clock to codec	Runtime	
S054	S54	SATA_ACT#	SATA	O OD CMOS	3V3		SATA Activity Indicator	Runtime	Shall be able to sink 24mA or more Carrier LED current

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S055	S55	USB5_EN_OC#	USB5	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 5	Standby	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
S056	S56	ESPI_IO_2 / QSPI_IO_2	QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S056	S56	ESPI_IO_2 / QSPI_IO_2	eSPI	I/O CMOS	1V8		ESPI Master Data Input / Output	Standby	
S057	S57	ESPI_IO_3 / QSPI_IO_3	QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S057	S57	ESPI_IO_3 / QSPI_IO_3	eSPI	I/O CMOS	1V8		ESPI Master Data Input / Output	Standby	
S058	S58	ESPI_RESET#	eSPI	O CMOS	1V8		ESPI Reset	Standby	
S059	S59	USB5+	USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S060	S60	USB5-	USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S061	S61	GND	PWR GND						
S062	S62	USB3_SSTX+	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S063	S63	USB3_SSTX-	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S064	S64	GND	PWR GND						
S065	S65	USB3_SSRX+	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S066	S66	USB3_SSRX-	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S067	S67	GND	PWR GND						
S068	S68	USB3+	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S069	S69	USB3-	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S070	S70	GND	PWR GND						
S071	S71	USB2_SSTX+	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S072	S72	USB2_SSTX-	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S073	S73	GND	PWR GND						

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S074	S74	USB2_SSRX+	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S075	S75	USB2_SSRX-	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S076	S76	PCIE_B_RST#	PCIEB	O CMOS	3V3		PCIe Port B reset output	Runtime	
S077	S77	PCIE_C_RST#	PCIEC	O CMOS	3V3		PCIe Port C reset output	Runtime	
S078	S78	PCIE_C_RX+ / SERDES_1_RX+	PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S078	S78	PCIE_C_RX+ / SERDES_1_RX+	SERDES1	I PCIE			Differential SERDES 1 Receive Data Pair	Runtime	
S079	S79	PCIE_C_RX- / SERDES_1_RX-	PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S079	S79	PCIE_C_RX- / SERDES_1_RX-	SERDES1	I PCIE			Differential SERDES 1 Receive Data Pair	Runtime	
S080	S80	GND	PWR GND						
S081	S81	PCIE_C_TX+ / SERDES_1_TX+	PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S081	S81	PCIE_C_TX+ / SERDES_1_TX+	SERDES1	O PCIE			Differential SERDES 1 Transmit Data Pair	Runtime	Series AC coupled on Module
S082	S82	PCIE_C_TX- / SERDES_1_TX-	PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S082	S82	PCIE_C_TX- / SERDES_1_TX-	SERDES1	O PCIE			Differential SERDES 1 Transmit Data Pair	Runtime	Series AC coupled on Module
S083	S83	GND	PWR GND						
S084	S84	PCIE_B_REFCK+	PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	
S085	S85	PCIE_B_REFCK-	PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	
S086	S86	GND	PWR GND						
S087	S87	PCIE_B_RX+	PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S088	S88	PCIE_B_RX-	PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S089	S89	GND	PWR GND						
S090	S90	PCIE_B_TX+	PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S091	S91	PCIE_B_TX-	PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S092	S92	GND	PWR GND						
S093	S93	DP0_LANE0+	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S094	S94	DP0_LANE0-	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S095	S95	DP0_AUX_SEL	DP0++	I CMOS	1V8	PD 1M	Auxiliary Selection	Runtime	
S096	S96	DP0_LANE1+	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S097	S97	DP0_LANE1-	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S098	S98	DP0_HPD	DP0++	I CMOS	1V8	PD 1M	DP Hot Plug Detect Input	Runtime	
S099	S99	DP0_LANE2+	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S100	S100	DP0_LANE2-	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S101	S101	GND	PWR GND						
S102	S102	DP0_LANE3+	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S103	S103	DP0_LANE3-	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S104	S104	USB3_OTG_ID	USB3	I CMOS	3V3		Input Pin to Announce OTG Device Insertion on USB 3.2 Port	Standby	
S105	S105	DP0_AUX+	DP0++	I/O DP	3V3	PD 100k	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S106	S106	DP0_AUX-	DP0++	I/O DP	3V3	PU 100k	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S107	S107	LCD1_BKLT_EN	eDP1	O CMOS	1V8		Secondary LVDS Channel Backlight Enable	Runtime	
S107	S107	LCD1_BKLT_EN	DSI1	O CMOS	1V8		Secondary Panel Backlight Enable	Runtime	
S107	S107	LCD1_BKLT_EN	LVDS1	O CMOS	1V8		Secondary Panel Backlight Enable	Runtime	
S108	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S108	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	eDP1	I/O DP			Secondary Bidirectional Channel used for Link Management and Device Control	Runtime	
S108	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Clock Lines	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S109	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S109	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	eDP1	I/O DP			Secondary Bidirectional Channel used for Link Management and Device Control	Runtime	
S109	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Clock Lines	Runtime	
S110	S110	GND	PWR GND						
S111	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S111	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S111	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S112	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S112	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S112	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S113	S113	eDP1_HPD / DSI1_TE	DSI1	I CMOS	1V8	PD 1M	Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	Runtime	
S113	S113	eDP1_HPD / DSI1_TE	eDP1	I CMOS	1V8	PD 1M	Secondary DSI Panel Tearing Effect Signal	Runtime	
S114	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S114	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S114	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S115	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S115	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S115	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S116	S116	LCD1_VDD_EN	DSI1	O CMOS	1V8		Secondary Panel Power Enable	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S116	S116	LCD1_VDD_EN	eDP1	O CMOS	1V8		Secondary Panel Power Enable	Runtime	
S116	S116	LCD1_VDD_EN	LVDS1	O CMOS	1V8		Secondary LVDS Channel Power Enable	Runtime	
S117	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S117	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S117	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S118	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S118	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S118	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S119	S119	GND	PWR GND						
S120	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S120	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S120	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S121	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S121	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	eDP1	O DP			Secondary 4-Lane eDP Differential Pair Data Lines	Runtime	
S121	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1	O LVDS			Secondary LVDS Channel Differential Pair Data Lines	Runtime	
S122	S122	LCD1_BKLT_PWM	DSI1	O CMOS	1V8		Secondary Panel Brightness Control	Runtime	
S122	S122	LCD1_BKLT_PWM	eDP1	O CMOS	1V8		Secondary Panel Brightness Control	Runtime	
S122	S122	LCD1_BKLT_PWM	LVDS1	O CMOS	1V8		Secondary LVDS Channel Brightness Control	Runtime	
S123	S123	GPIO13	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 13 Preferred Output	Runtime	
S124	S124	GND	PWR GND						
S125	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S125	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S125	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S126	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S126	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S126	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S127	S127	LCD0_BKLT_EN	DSI0	O CMOS	1V8		Primary Panel Backlight Enable	Runtime	
S127	S127	LCD0_BKLT_EN	eDP0	O CMOS	1V8		Primary Panel Backlight Enable	Runtime	
S127	S127	LCD0_BKLT_EN	LVDS0	O CMOS	1V8		Primary LVDS Channel Backlight Enable	Runtime	
S128	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S128	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S128	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S129	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S129	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S129	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S130	S130	GND	PWR GND						
S131	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S131	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S131	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S132	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S132	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S132	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S133	S133	LCD0_VDD_EN	DSI0	O CMOS	1V8		Primary Panel Power Enable	Runtime	
S133	S133	LCD0_VDD_EN	eDP0	O CMOS	1V8		Primary Panel Power Enable	Runtime	
S133	S133	LCD0_VDD_EN	LVDS0	O CMOS	1V8		Primary LVDS Channel Power Enable	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S134	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S134	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	eDP0	I/O DP			Primary Bidirectional Channel used for Link Management and Device Control	Runtime	
S134	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Clock Lines	Runtime	
S135	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S135	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	eDP0	I/O DP			Primary Bidirectional Channel used for Link Management and Device Control	Runtime	
S135	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Clock Lines	Runtime	
S136	S136	GND	PWR GND						
S137	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S137	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S137	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S138	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S138	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	eDP0	O DP			Primary 4-Lane eDP Differential Pair Data Lines	Runtime	
S138	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0	O LVDS			Primary LVDS Channel Differential Pair Data Lines	Runtime	
S139	S139	I2C_LCD_CK	DSI	I\O OD CMOS	1V8	PU 2K2	I2C clock to read LCD display EDID EEPROMs	Runtime	
S139	S139	I2C_LCD_CK	eDP	I\O OD CMOS	1V8	PU 2K2	DDC Clock Line Used for Flat Panel Detection and Control	Runtime	
S139	S139	I2C_LCD_CK	LVDS	I\O OD CMOS	1V8	PU 2K2	I2C clock to read LCD display EDID EEPROMs	Runtime	
S140	S140	I2C_LCD_DAT	DSI	I\O OD CMOS	1V8	PU 2K2	DDC Data Line Used for Flat Panel Detection and Control	Runtime	
S140	S140	I2C_LCD_DAT	eDP	I\O OD CMOS	1V8	PU 2K2	I2C Data to Read LCD Display EDID EEPROMs	Runtime	
S140	S140	I2C_LCD_DAT	LVDS	I\O OD CMOS	1V8	PU 2K2	DDC Data Line Used for Flat Panel Detection and Control	Runtime	
S141	S141	LCD0_BKLT_PWM	DSI0	O CMOS	1V8		Primary Panel Brightness Control	Runtime	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S141	S141	LCD0_BKLT_PWM	eDP0	O CMOS	1V8		Primary Panel Brightness Control	Runtime	
S141	S141	LCD0_BKLT_PWM	LVDS0	O CMOS	1V8		Primary LVDS Channel Brightness Control	Runtime	
S142	S142	GPIO12	GPIO	I/O CMOS	1V8	PU 470K	GPIO Pin 12 Preferred Output	Runtime	
S143	S143	GND	PWR GND						
S144	S144	eDP0_HPD / DSI0_TE	DSI0	I CMOS	1V8	PD 1M	Primary DSI Panel Tearing Effect Signal	Runtime	
S144	S144	eDP0_HPD / DSI0_TE	eDP0	I CMOS	1V8	PD 1M	Detection of Hot Plug / Unplug of Primary eDP Display and Notification of the Link Layer	Runtime	
S145	S145	WDT_TIME_OUT#	WATCHDOG	O CMOS	1V8		Watch-Dog-Timer Output, low active	Runtime	
S146	S146	PCIE_WAKE#	PCIE	I OD CMOS	3V3	PU 10K	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	Standby	
S147	S147	VDD_RTC	PWR RTC		2V…3.25V				
S148	S148	LID#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	Standby	
S149	S149	SLEEP#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Standby	
S150	S150	VIN_PWR_BAD#	MANAGEMENT	I OD CMOS	VDD_IN	PU 10K	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.		
S151	S151	CHARGING#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	Standby/Sleep	

Pin #	Pin #	Name	Group	I/O Type	I/O Level	PU / PD	Description	Power Domain	Comments
S152	S152	CHARGER_PRSNT#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Held low by Carrier if DC input for battery charger is present	Standby/Sleep	
S153	S153	CARRIER_STBY#	MANAGEMENT	O CMOS	1V8		The Module shall drive this signal low when the system is in a standby power state.	Standby	
S154	S154	CARRIER_PWR_ON	MANAGEMENT	O CMOS	1V8		Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	Standby	
S155	S155	FORCE_RECOV#	BOOT	I OD CMOS	1V8	PU 10K	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	Standby	
S156	S156	BATLOW#	MANAGEMENT	I OD CMOS	1V8…5V	PU 10K	Battery low indication to Module. Carrier to float the line in inactive state.	Standby/Sleep	
S157	S157	TEST#	MANAGEMENT	I OD CMOS	1V8…5V	PU Vendor specific	Held Low by Carrier to Invoke Module Vendor Specific Test Functions	Standby/Sleep	
S158	S158	GND	PWR GND						

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