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Retimer

Производители

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Микросхемы

TI DS280DF810

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
1	RX0P	C15	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
2	RX0N	B15	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
3	RX1P	B13	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
4	RX1N	A13	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
5	RX2P	B11	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
6	RX2N	A11	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
7	RX3P	B9	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
8	RX3N	A9	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
9	RX4P	B7	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
10	RX4N	A7	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
11	RX5P	B5	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
12	RX5N	A5	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
13	RX6P	B3	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
14	RX6N	A3	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
15	RX7P	C1	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
16	RX7N	B1	Input		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
17	TX0P	G15	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
18	TX0N	H15	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
19	TX1P	H13	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
20	TX1N	J13	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
21	TX2P	H11	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
22	TX2N	J11	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
23	TX3P	H9	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
24	TX3N	J9	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
25	TX4P	H7	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
26	TX4N	J7	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
27	TX5P	H5	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
28	TX5N	J5	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
29	TX6P	H3	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
30	TX6N	J3	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
31	TX7P	G1	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
32	TX7N	H1	Output		None	HIGH SPEED DIFFERENTIAL I/Os	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
33	CAL_CLK_IN	E1	Input	2.5 V CMOS	Weak pull-down	CALIBRATION CLOCK PINS	25 MHz (±100 PPM) 2.5 V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. Used to calibrate VCO frequency range. This clock is not used to recover data.
34	CAL_CLK_OUT	E15	Output	2.5 V CMOS	None	CALIBRATION CLOCK PINS	2.5 V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
35	ADDR0	D13	Input	2.5 V 4-level	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD Refer to Device SMBus Address for more information.
36	ADDR1	E13	Input	2.5 V 4-level	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD Refer to Device SMBus Address for more information.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
37	EN_SMB	E3	Input	2.5 V 4-level	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	Four-level 2.5 V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED, TI test mode. R: 10 kΩ to GND - RESERVED, TI test mode F: Float - SMBus Master Mode 1: 1 kΩ to VDD - SMBus Slave Mode
38	SDA	E12	I/O	3.3 V LVCMOS, Open Drain	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	SMBus data input and open drain output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
39	SDC	F12	I/O	3.3 V LVCMOS, Open Drain	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	SMBus clock input and open drain clock output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
40	READ_EN_N	F13	Input	3.3 V LVCMOS	Weak pull-up	SYSTEM MANAGEMENT BUS (SMBUS) PINS	SMBus Master Mode (EN_SMB=Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. This pin is 3.3 V tolerant. SMBus Slave Mode (EN_SMB=1): When asserted low, this causes the device to be held in reset (I2C state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus Slave Mode. This pin is 3.3 V tolerant.
41	ALL_DONE_N	D3	Output	LVCMOS	None	SYSTEM MANAGEMENT BUS (SMBUS) PINS	Indicates the completion of a valid EEPROM register load operation when in SMBus Master Mode (EN_SMB=Float): High = External EEPROM load failed or incomplete Low = External EEPROM load successful and complete When in SMBus slave mode (EN_SMB=1), this output reflects the status of READ_EN_N input.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
42	INT_N	F3	Output	LVCMOS, Open-Drain	None	MISCELLANEOUS PINS	Open-drain 3.3 V tolerant active-low interrupt output. It pulls low when an interrupt occurs. The events which trigger an interrupt are programmable through SMBus registers. This pin can be connected in a wired-OR fashion with other device's interrupt pin. A single pull-up resistor in the 2 kΩ to 5 kΩ range is adequate for the entire INT_N net.
43	TEST0	E2	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (max) output.
44	TEST1	E14	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (max) output.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
45	TEST4	F4	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin should be tied to GND or left floating.
46	TEST5	E4	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5 V (max) output.
47	TEST6	D4	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5 V (max) output.
48	TEST7	D12	Input	LVCMOS	Weak pull-up	MISCELLANEOUS PINS	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5 V (max) output.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
49	VDD	D6	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
50	VDD	D8	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
51	VDD	D10	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
52	VDD	E5	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
53	VDD	E6	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
54	VDD	E7	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
55	VDD	E8	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
56	VDD	E9	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
57	VDD	E10	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
58	VDD	F6	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
59	VDD	F8	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.
60	VDD	F10	Power	2.5 V	None	POWER	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 µF capacitors and two 1 µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a lowresistance path to the board VDD plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
61	GND	A1	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
62	GND	A2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
63	GND	A4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
64	GND	A6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
65	GND	A8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
66	GND	A10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
67	GND	A12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
68	GND	A14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
69	GND	A15	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
70	GND	B2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
71	GND	B4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
72	GND	B6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
73	GND	B8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
74	GND	B10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
75	GND	B12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
76	GND	B14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
77	GND	C2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
78	GND	C3	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
79	GND	C4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
80	GND	C5	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
81	GND	C6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
82	GND	C7	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
83	GND	C8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
84	GND	C9	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
85	GND	C10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
86	GND	C11	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
87	GND	C12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
88	GND	C13	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
89	GND	C14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
90	GND	D1	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
91	GND	D2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
92	GND	D5	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
93	GND	D7	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
94	GND	D9	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
95	GND	D11	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
96	GND	D14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
97	GND	D15	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
98	GND	E11	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
99	GND	F1	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
100	GND	F2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
101	GND	F5	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
102	GND	F7	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
103	GND	F9	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
104	GND	F11	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
105	GND	F14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
106	GND	F15	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
107	GND	G2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
108	GND	G3	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
109	GND	G4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
110	GND	G5	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
111	GND	G6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
112	GND	G7	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
113	GND	G8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
114	GND	G9	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
115	GND	G10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
116	GND	G11	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
117	GND	G12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
118	GND	G13	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
119	GND	G14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
120	GND	H2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
121	GND	H4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
122	GND	H6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
123	GND	H8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
124	GND	H10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
125	GND	H12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
126	GND	H14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
127	GND	J1	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
128	GND	J2	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
129	GND	J4	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
130	GND	J6	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
131	GND	J8	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
132	GND	J10	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

NN	PIN NAME	PIN NO.	TYPE	Voltage	INTERNAL PULL-UP/ PULL-DOWN	GROUP	DESCRIPTION
133	GND	J12	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
134	GND	J14	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.
135	GND	J15	Power		None	POWER	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.