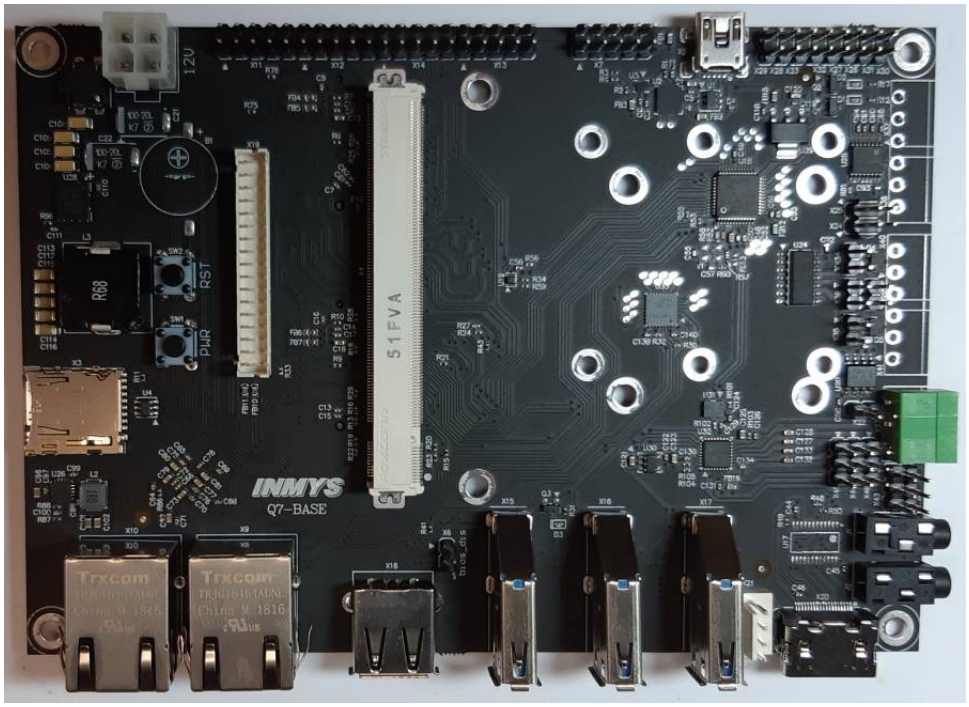
Содержание

NMS-Q7-EVM V1.1 ds-en



Introduction

All connections with the external world come through this motherboard, which provide also the required voltage to modules, deriving it from its power supply source.

This board implement the routing of the interface signals Qseven module to external standard connectors.

Technical Specifications

Main technical specifications

Video Interfaces	HDMI interface
Video Resolutions	HDMI resolution up to 4k@60Hz
Mass Storage	1 x S-ATA channel (M.2 connector)
USB	- 3 x USB 3.0 - 1 x USB 2.0 - 1 x mini USB (USB to UART console)
Networking	- Gigabit Ethernet interface (from Q7 SOM Ethernet PHY) - Gigabit Ethernet interface (from onboard Intel WGI210ITSLJX PCIe Gigabit Ethernet PHY)
Audio	- Audio 3.5 mm jack (Line in\Mic in) - Audio 3.5 mm jack (Line out\Headphones)
PCI Express	2 x PCI-e 1x: - one routed to M.2 Connector - one routed to Intel WGI210ITSLJX PCIe Gigabit Ethernet PHY
Serial Ports	1 x Serial port (RS-232/RS-485/RS-422) 1 x Debug console (UART to USB)

Other Interfaces	- 1 x CAN interface - 2 x I2C interface - 1 x SPI interface - 1 x LPC interface (8 GPIO)
Power supply voltage	+12 VDC
Power consumption	**TBD**
Operating temperature	-40°C...+85°C
Dimensions:	147 x 101.60 mm

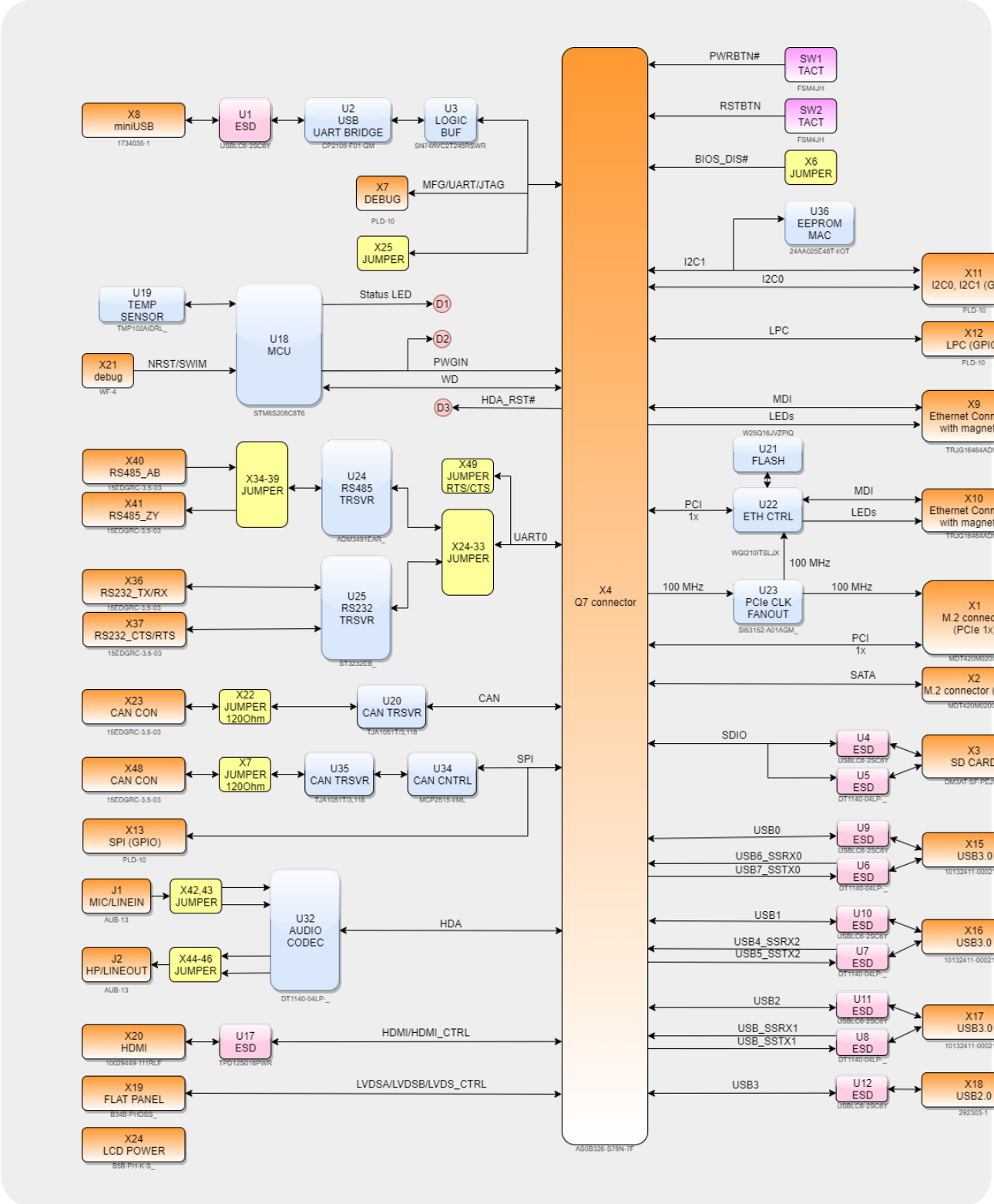
Electrical Specifications

For correct operation this board need external +12VDC power supply.

Input Voltage: 12V.

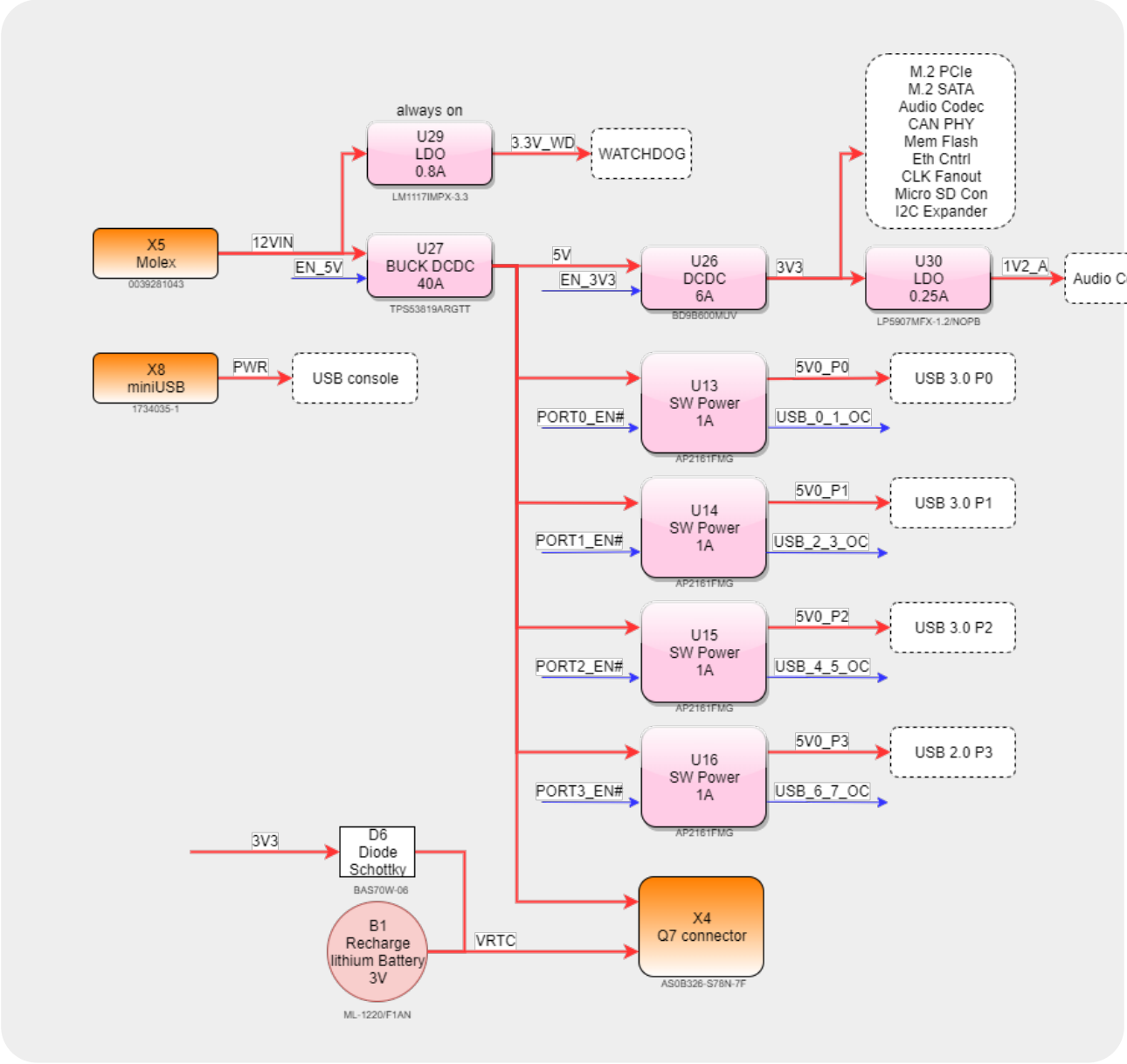
All remaining voltages needed for board’s working are generated internally from +12VDC power rail.

Block Diagram



Q7Base block diagram

Power tree

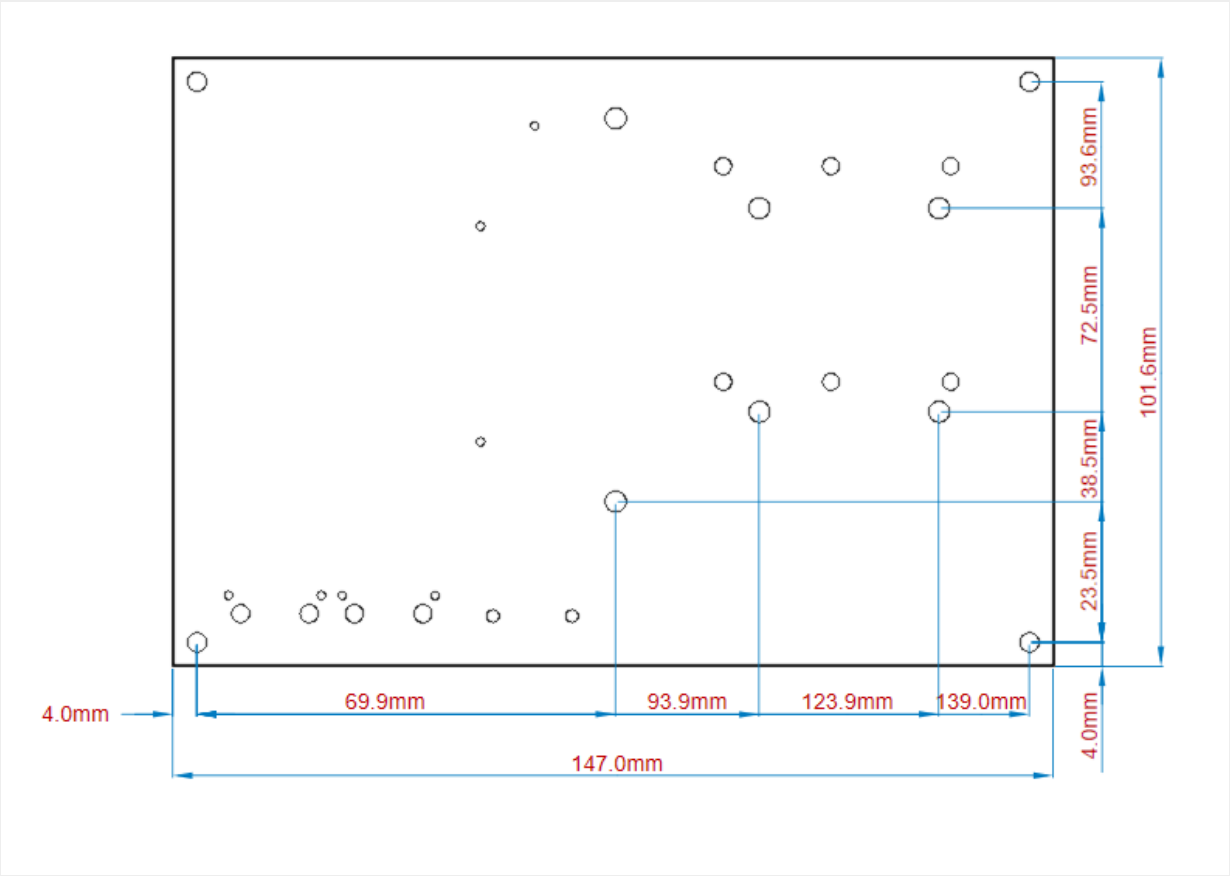


Q7Base power tree

Mechanical Specifications

Board dimensions are: 147 x 101.60 mm.

Printed circuit of the board is made of 6 layers, some of them are ground planes, for disturbance rejection.



Q7Base mechanical dimensions

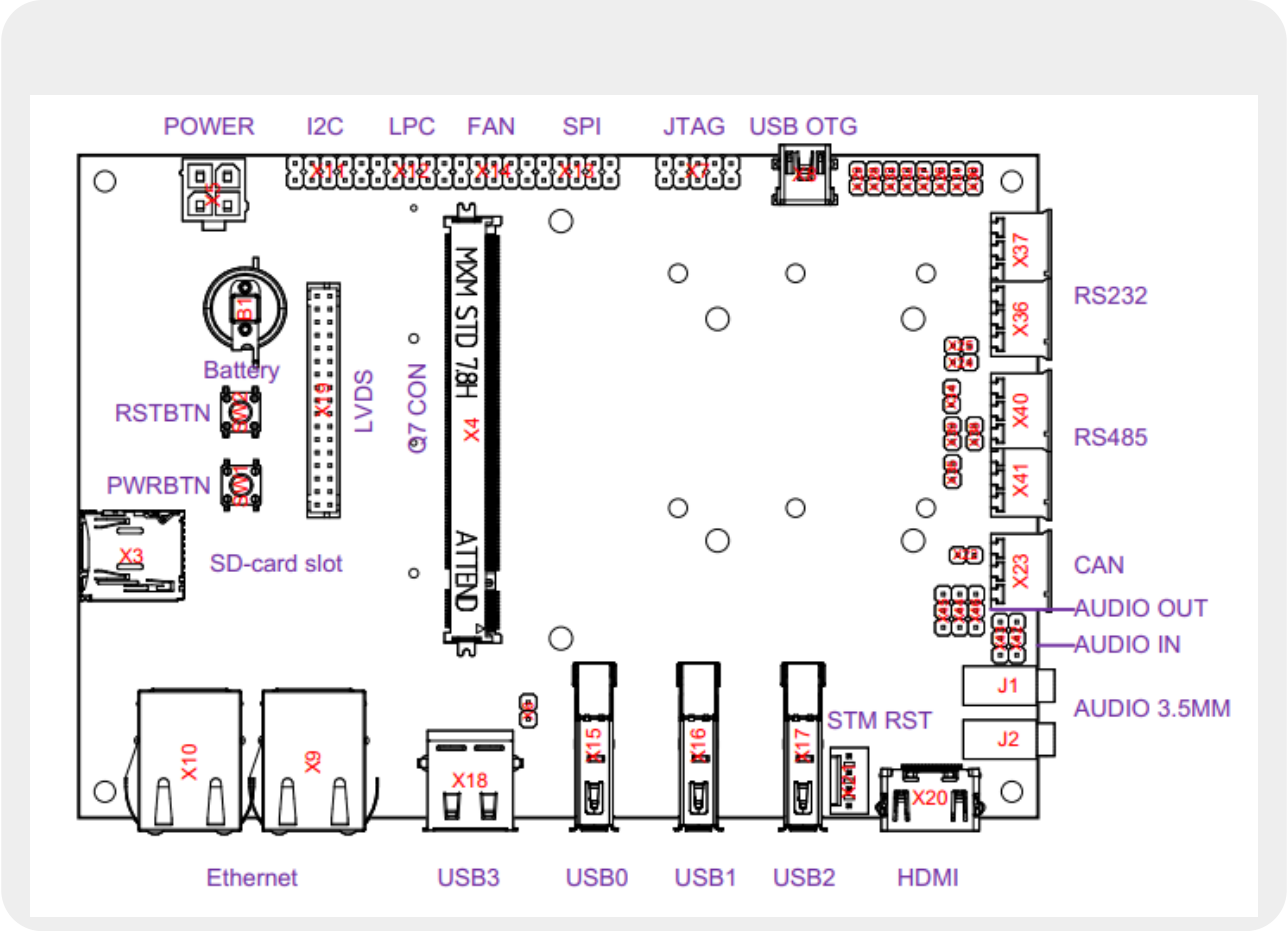
Connectors

Introduction

Over current protection, power supply filtering and ESD protection is provided.

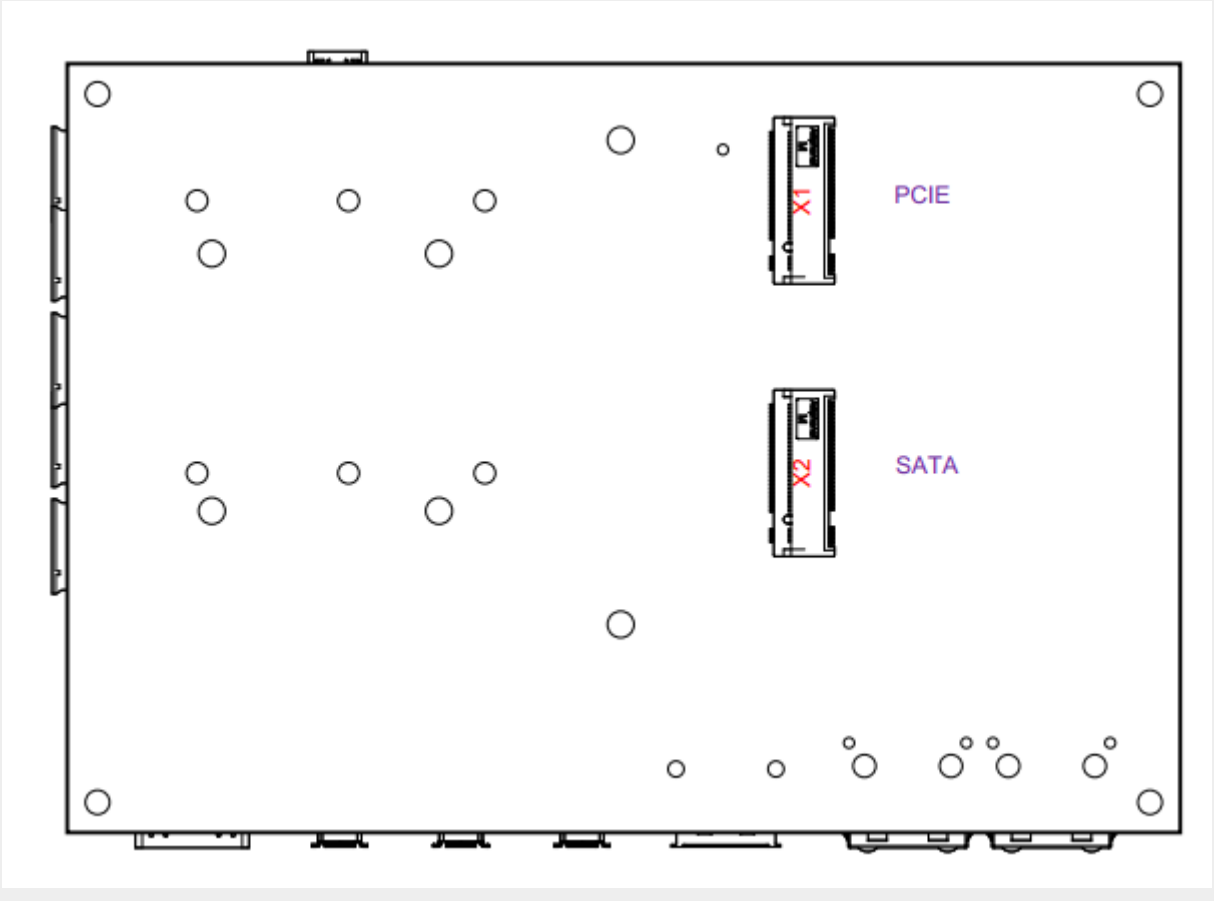
Connector Locations

Top View



Q7Base top components view

Bottom View



Q7Base bot components view

Connectors description

Power in connector

Power connector

Function	Power	
Location	X5	
P/N	0039281043 Molex	
Pinout	**Pin**	**Description**
	1	GND
	2	GND
	3	12VIN
	4	12VIN

Qseven® Connector

Qseven connector

Function	Qseven Gen 2.0 Connector
Location	X4
P/N	AS0B326-S78N-7F MFG FOXCONN
Pinout	see the table below

Qseven connector pinout

Pins	Name (Bottom side row)	Signal group	Type	Comments	Pins	Name (Top side row)	Signal group	Type	Comments
1	GND		PWR		2	GND		PWR	
3	GBE_MDI3-	GBE	IO		4	GBE_MDI2-	GBE	IO	
5	GBE_MDI3+	GBE	IO		6	GBE_MDI2+	GBE	IO	
7	GBE_LINK100#	GBE	I	NC	8	GBE_LINK1000#	GBE	I	NC
9	GBE_MDI1-	GBE	IO		10	GBE_MDI0-	GBE	IO	
11	GBE_MDI1+	GBE	IO		12	GBE_MDI0+	GBE	IO	
13	GBE_LINK#	GBE	I		14	GBE_ACT#	GBE	I	
15	GBE_CTREF	GBE	I	NC	16	SUS_S5#	PWR_MGMT	I	NC
17	WAKE#	PWR_MGMT	O	PU	18	SUS_S3#	PWR_MGMT	I	NC
19	GPO0(SUS_STAT#)	PWR_MGMT	I		20	PWRBTN#	PWR_MGMT	O	PU
21	SLP_BTN#/GPII1	PWR_MGMT	O	PU	22	LID_BTN#/GPII0	PWR_MGMT	O	PU
23	GND		PWR		24	GND		PWR	
	KEY					KEY			
25	GND		PWR		26	PWGIN	PWR_MGMT	O	PD
27	BATLOW#/GPII2	PWR_MGMT	O	PU	28	RSTBTN#	PWR_MGMT	O	PU
29	SATA0_TX+	SATA	I		30	SATA1_TX+	SATA	I	NC
31	SATA0_TX-	SATA	I		32	SATA1_TX-	SATA	I	NC
33	SATA_ACT#	SATA	I	NC	34	GND		PWR	
35	SATA0_RX+	SATA	O		36	SATA1_RX+	SATA	O	NC
37	SATA0_RX-	SATA	O		38	SATA1_RX-	SATA	O	NC
39	GND		PWR		40	GND		PWR	
41	BIOS_DIS#/BOOT_ALT#	BOOT	O	PU	42	SDIO_CLK#	SDIO	I	
43	SDIO_CD#	SDIO	IO		44	reserved (SDIO_LED)			
45	SDIO_CMD	SDIO	IO		46	SDIO_WP	SDIO	IO	PD
47	SDIO_PWR#	SDIO	I	NC	48	SDIO_DAT1	SDIO	IO	
49	SDIO_DAT0	SDIO	IO		50	SDIO_DAT3	SDIO	IO	
51	SDIO_DAT2	SDIO	IO		52	reserved (SDIO_DAT5)			
53	reserved (SDIO_DAT4)				54	reserved (SDIO_DAT7)			
55	reserved (SDIO_DAT6)				56	USB_OTG_PEN (RSVD)	USB	I	NC

Pins	Name (Bottom side row)	Signal group	Type	Comments	Pins	Name (Top side row)	Signal group	Type	Comments
57	GND		PWR		58	GND		PWR	
59	HDA_SYNC/I2S_WS	AUDIO	I		60	SMB_CLK/GP1_I2C_CLK	MISC	IO	
61	HDA_RST#/I2S_RST#	AUDIO	I		62	SMB_DAT/GP1_I2C_DAT	MISC	IO	
63	HDA_BITCLK/I2S_CLK	AUDIO	I		64	SMB_ALERT#	MISC	IO	
65	HDA_SDI/I2S_SDI	AUDIO	O		66	GP0_I2C_CLK (I2C_CLK)	MISC	IO	
67	HDA_SDO/I2S_SDO	AUDIO	I		68	GP0_I2C_DAT (I2C_DAT)	MISC	IO	
69	THRM#	MISC	O	PU	70	WDTRIG#	MISC	O	PU
71	THRMTRIP#	MISC	I		72	WDOUT	MISC	I	
73	GND		PWR		74	GND		PWR	
75	USB_P7-/USB_SSTX0-	USB	IO		76	USB_P6-/USB_SSRX0-	USB	IO	
77	USB_P7+/USB_SSTX0+	USB	IO		78	USB_P6+/USB_SSRX0+	USB	IO	
79	USB_6_7_OC#	USB	O		80	USB_4_5_OC#	USB	O	
81	USB_P5-/USB_SSTX2-	USB	IO		82	USB_P4-/USB_SSRX2-	USB	IO	
83	USB_P5+/USB_SSTX2+	USB	IO		84	USB_P4+/USB_SSRX2+	USB	IO	
85	USB_2_3_OC#	USB	O		86	USB_0_1_OC#	USB	O	
87	USB_P3-	USB	IO		88	USB_P2-	USB	IO	
89	USB_P3+	USB	IO		90	USB_P2+	USB	IO	
91	USB_VBUS (USB_CC)	USB	O	PU	92	USB_ID	USB	O	PD
93	USB_P1-	USB	IO		94	USB_P0-	USB	IO	
95	USB_P1+	USB	IO		96	USB_P0+	USB	IO	
97	GND		PWR		98	GND		PWR	
99	eDP0_TX0+/LVDS_A0+	LVDS/eDP	I		100	eDP1_TX0+/LVDS_B0+	LVDS/eDP	I	
101	eDP0_TX0-/LVDS_A0-	LVDS/eDP	I		102	eDP1_TX0-/LVDS_B0-	LVDS/eDP	I	
103	eDP0_TX1+/LVDS_A1+	LVDS/eDP	I		104	eDP1_TX1+/LVDS_B1+	LVDS/eDP	I	
105	eDP0_TX1-/LVDS_A1-	LVDS/eDP	I		106	eDP1_TX1-/LVDS_B1-	LVDS/eDP	I	
107	eDP0_TX2+/LVDS_A2+	LVDS/eDP	I		108	eDP1_TX2+/LVDS_B2+	LVDS/eDP	I	
109	eDP0_TX2-/LVDS_A2-	LVDS/eDP	I		110	eDP1_TX2-/LVDS_B2-	LVDS/eDP	I	
111	LVDS_PPEN	LVDS/eDP	I		112	LVDS_BLEN	LVDS/eDP	I	
113	eDP0_TX3+/LVDS_A3+	LVDS/eDP	I		114	eDP1_TX3+/LVDS_B3+	LVDS/eDP	I	
115	eDP0_TX3-/LVDS_A3-	LVDS/eDP	I		116	eDP1_TX3-/LVDS_B3-	LVDS/eDP	I	
117	GND		PWR		118	GND		PWR	
119	eDP0_AUX+/LVDS_A_CLK+	LVDS	I		120	eDP1_AUX+/LVDS_B_CLK+	LVDS	IO	
121	eDP0_AUX-/LVDS_A_CLK-	LVDS	I		122	eDP1_AUX-/LVDS_B_CLK-	LVDS	IO	
123	LVDS_BLT_CTRL/ GP_PWM_OUT0	LVDS/eDP	I		124	GP_1-Wire_Bus/ HDMI_CEC (RSVD)	HDMI/DP	IO	
125	LVDS_DID_DAT/GP_I2C_DAT	LVDS	IO		126	eDP0_HPD#/LVDS_BLC_DAT	LVDS	IO	
127	LVDS_DID_CLK/GP_I2C_CLK	LVDS	IO		128	eDP1_HPD#/LVDS_BLC_CLK	LVDS	IO	
129	CAN0_TX	CAN	I		130	CAN0_RX	CAN	O	
131	DP_LANE3+/TMDS_CLK+ (SDVO_BCLK+)	HDMI/DP	I		132	USB_SSTX1- (SDVO_INT+)	USB	I	
133	DP_LANE3-/TMDS_CLK- (SDVO_BCLK-)	HDMI/DP	I		134	USB_SSTX1+ (SDVO_INT-)		I	
135	GND		PWR		136	GND		PWR	
137	DP_LANE1+/TMDS_LANE1+ (SDVO_GREEN+)	HDMI/DP	I		138	DP_AUX+ (SDVO_FLDSTALL+)	DP	IO	NC
139	DP_LANE1-/TMDS_LANE1- (SDVO_GREEN-)	HDMI/DP	I		140	DP_AUX- (SDVO_FLDSTALL-)	DP	IO	NC
141	GND		PWR		142	GND		PWR	
143	DP_LANE2+/TMDS_LANE0+ (SDVO_BLUE+)	HDMI/DP	I		144	USB_SSRX1- (SDVO_TVCLKIN+)	USB	O	
145	DP_LANE2-/TMDS_LANE0- (SDVO_BLUE-)	HDMI/DP	I		146	USB_SSRX1+ (SDVO_TVCLKIN-)	USB	O	
147	GND		PWR		148	GND		PWR	
149	DP_LANE0+/TMDS_LANE2+ (SDVO_RED+)	HDMI/DP	I		150	HDMI_CTRL_DAT (SDVO_CTRL_DAT)	HDMI/DP	IO	
151	DP_LANE0-/TMDS_LANE2- (SDVO_RED-)	HDMI/DP	I		152	HDMI_CTRL_CLK (SDVO_CTRL_CLK)	HDMI/DP	IO	
153	HDMI_HPD#	HDMI/DP	O	PU	154	DP_HPD#	DP	O	NC
155	PCIE_CLK_REF+	PCI-E	I		156	PCIE_WAKE#	PCI-E	O	

Pins	Name (Bottom side row)	Signal group	Type	Comments	Pins	Name (Top side row)	Signal group	Type	Comments
157	PCIE_CLK_REF-	PCI-E	I		158	PCIE_RST#	PCI-E	I	
159	GND		PWR		160	GND		PWR	
161	PCIE3_TX+	PCI-E	I	NC	162	PCIE3_RX+	PCI-E	O	NC
163	PCIE3_TX-	PCI-E	I	NC	164	PCIE3_RX-	PCI-E	O	NC
165	GND		PWR		166	GND		PWR	
167	PCIE2_TX+	PCI-E	I	NC	168	PCIE2_RX+	PCI-E	O	NC
169	PCIE2_TX-	PCI-E	I	NC	170	PCIE2_RX-	PCI-E	O	NC
171	UART0_TX (EXCD0_PERST#)	UART	I		172	UART0_RTS# (EXCD1_PERST#)	UART	I	
173	PCIE1_TX+	PCI-E	I		174	PCIE1_RX+	PCI-E	O	
175	PCIE1_TX-	PCI-E	I		176	PCIE1_RX-	PCI-E	O	
177	UART0_RX (EXCD0_CPPE#)	UART	O		178	UART0_CTS# (EXCD1_CPPE#)	UART	O	
179	PCIE0_TX+	PCI-E	I		180	PCIE0_RX+	PCI-E	O	
181	PCIE0_TX-	PCI-E	I		182	PCIE0_RX-	PCI-E	O	
183	GND		PWR		184	GND		PWR	
185	LPC_AD0/GPIO0	LPC	IO		186	LPC_AD1/GPIO1	LPC	IO	
187	LPC_AD2/GPIO2	LPC	IO		188	LPC_AD3/GPIO3	LPC	IO	
189	LPC_CLK/GPIO4	LPC	IO		190	LPC_FRAME#/GPIO5	LPC	IO	
191	SERIRQ/GPIO6	LPC	IO		192	LPC_LDRQ#/GPIO7	LPC	IO	
193	VCC_RTC		O		194	SPKR/GP_PWM_OUT2		I	
195	FAN_T_IN/GP_TIMER_IN	MISC	O		196	FAN_OUT/GP_PWM_OUT1	MISC	I	
197	GND		PWR		198	GND		PWR	
199	SPI_MOSI	SPI	I		200	SPI_CS0#	SPI	I	
201	SPI_MISO	SPI	O		202	SPI_CS1#	SPI	I	
203	SPI_SCK	SPI	I		204	MFG_NC4		O	
205	VCC_5V_SB		O		206	VCC_5V_SB		O	
207	MFG_NC0	MFG	O		208	MFG_NC2	MFG	O	
209	MFG_NC1	MFG	I		210	MFG_NC3	MFG	O	
211	NC (VCC)				212	NC (VCC)			
213	NC (VCC)				214	NC (VCC)			
215	NC (VCC)				216	NC (VCC)			
217	NC (VCC)				218	NC (VCC)			
219	VCC		O		220	VCC		O	
221	VCC		O		222	VCC		O	
223	VCC		O		224	VCC		O	
225	VCC		O		226	VCC		O	
227	VCC		O		228	VCC		O	
229	VCC		O		230	VCC		O	

PCI Express interface signals

Q7_Base can offer externally four PCI Express lane, which are directly managed by external Q7-module.
PCI express Gen 3.0 (8Gbps) is supported.
Here following the signals involved in PCI express management:

Q7 PCIe signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
PCIE0_TX+	179	in		PCI Express lane #0, Transmitting Input Differential pair.	
PCIE0_TX-	181				
PCIE0_RX+	180	out		PCI Express lane #0, Receiving Output Differential pair.	
PCIE0_RX-	182				

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
PCIE1_TX+	173	in		PCI Express lane #1, Transmitting Input Differential pair.	
PCIE1_TX-	175				
PCIE1_RX+	174	out		PCI Express lane #1, Receiving Output Differential pair.	
PCIE1_RX-	176				
PCIE2_TX+	167	in		PCI Express lane #2, Transmitting Input Differential pair.	
PCIE2_TX-	169				
PCIE2_RX+	168	out		PCI Express lane #2, Receiving Output Differential pair.	
PCIE2_RX-	170				
PCIE3_TX+	161	in		PCI Express lane #3, Transmitting Input Differential pair.	
PCIE3_TX-	163				
PCIE3_RX+	162	out		PCI Express lane #3, Receiving Output Differential pair.	
PCIE3_RX-	164				
PCIE_CLK_REF+	155	in		PCI Express Reference Clock for Lanes 0 to 3, Differential Pair.	
PCIE_CLK_REF-	157				
PCIE_WAKE#	156	out	3V3	Wake-up (output) signal to the system on external Q7-module. It is connected to the Ethernet Controller WGI210ITSLJX_ (U22.16) through 0 Ohm resistor (R70), for the possibility of disconnection.	
PCIE_RST#	158	in	3V3	Input Reset Signal that is sent from external Q7-module to the Ethernet Controller (U22.17) and to the connector MDT420M02001 (X1.50).	

UART interface signals

Q7-Base offers one UART interface.
Here following the signals related to UART interface:

Q7 Uart signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
UART0_TX	171	in	3V3	UART Interface, Serial data Transmit line.	
UART0_RX	177	out	3V3	UART Interface, Serial data Receive line.	
UART0_RTS#	172	in	3V3	UART Interface, Handshake signal, Request to Send line.	
UART0_CTS#	178	out	3V3	UART Interface, Handshake signal, Clear to Send line.	

Gigabit Ethernet signals

Here following the signals involved in PCI express management

Q7 ethernet signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
GBE_MDI0+	12	in/out		Media Dependent Interface (MDI) I/O differential pair #0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	
GBE_MDI0-	10				
GBE_MDI1+	11	in/out		Media Dependent Interface (MDI) I/O differential pair #1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	
GBE_MDI1-	9				
GBE_MDI2+	6	in/out		Media Dependent Interface (MDI) I/O differential pair #2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	
GBE_MDI2-	4				
GBE_MDI3+	5	in/out		Media Dependent Interface (MDI) I/O differential pair #3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	
GBE_MDI3-	3				
GBE_ACT#	14	in	3V3	Ethernet controller activity indicator.	
GBE_LINK#	13	in	3V3	Ethernet controller link indicator.	
GBE_LINK100#	7	in	3V3	Ethernet controller 100Mbps link indicator.	Not used.
GBE_LINK1000#	8	in	3V3	Ethernet controller 1Gbps link indicator.	Not used.
GBE_CTREF	15	in		Reference voltage for Ethernet channel 0 magnetics center tap.	

SATA signals

There are two SATA interface on Q7_Base, but it is available only one.
Here following the signals related to SATA interface:

Q7 SATA signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
SATA0_TX+	29	in		Serial ATA Channel #0 Transmit differential pair.	
SATA0_TX-	31				
SATA0_RX+	35	out		Serial ATA Channel #0 Receive differential pair.	
SATA0_RX-	37				
SATA_ACT#	33	in	3V3	Serial ATA Activity Led.	Not used.
SATA1_TX+	30	in		Serial ATA channel 1, Receive Input differential pair.	Not used.
SATA1_TX-	32				

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
SATA1_RX+	36	out		Serial ATA channel 1, Transmit Output differential pair.	Not used.
SATA1_RX-	38				

SDI/O interface signals

SDI/O port #1 can work in 1-bit and 4-bit.

Signals involved with SDI/O interface are the following:

Q7 SDIO signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
SDIO_CD#	43	in/out	3V3	Card Detect Output which signals that a SDIO Card is present.	
SDIO_CLK	42	in	3V3	Clock Line.	
SDIO_CMD	45	in/out	3V3	Command/Response line. Signal used to send command from Host (Q7 module) to the connected card (Q7_Base), and to send the response from the card to the Host.	
SDIO_LED	44	in	3V3	LED input signal.	Not used.
SDIO_WP	46	in/out	3V3 10kΩ pull-down	Write Protect bidirectional signal.	
SDIO_PWR#	47	in	3V3	SD power enable (It is used to drive an LED when there are transfers on SD Bus).	Not used.
SDIO_DAT[0÷7]	48-51	in/out	3V3	SDIO data bus. **SDIO_DAT0** signal is used for all communication modes. **SDIO_DAT[1÷3]** signals are required for 4-bit SDIO communication modes.	**SDIO_DAT[4÷7]** not used.

USB interface signals

Here following the signals related to USB interfaces.

Q7 USB signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
USB_P0+	96	in/out		Universal Serial Bus Port #0 differential pair.			
USB_P0-	94						

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
USB_P1+	95	in/out		Universal Serial Bus Port #1 differential pair.			
USB_P1-	93						
USB_P2+	90	in/out		Universal Serial Bus Port #2 differential pair.			
USB_P2-	88						
USB_P3+	89	in/out		Universal Serial Bus Port #3 differential pair.			
USB_P3-	87						
USB_P4+	84	in/out		Universal Serial Bus Port #4 differential pair.	USB_SSRX2+	USB Super Speed Port #2 receive differential pair.	out
USB_P4-	82				USB_SSRX2-		
USB_P5+	83	in/out		Universal Serial Bus Port #5 differential pair.	USB_SSTX2+	USB Super Speed Port #2 transmit differential pair.	in
USB_P5-	81				USB_SSTX2-		
USB_P6+	78	in/out		Universal Serial Bus Port #6 differential pair.	USB_SSRX0+	USB Super Speed Port #0 receive differential pair.	out
USB_P6-	76				USB_SSRX0-		
USB_P7+	77	in/out		Universal Serial Bus Port #7 differential pair.	USB_SSTX0+	USB Super Speed Port #0 transmit differential pair.	in
USB_P7-	75				USB_SSTX0-		
USB_SSRX1+	132	out		USB Super Speed Port #1 receive differential pair.			
USB_SSRX1-	134						
USB_SSTX1+	144	in		USB Super Speed Port #1 transmit differential pair.			
USB_SSTX1-	146						

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
USB_0_1_OC#	86	out	3V3	USB Over Current Detect Input. This pin used for overcurrent detection of USB Port#0 and #1.			
USB_2_3_OC#	85	out	3V3	USB Over Current Detect Input. This pin has to be used for overcurrent detection of USB Ports #2 and/or #3.			
USB_4_5_OC#	80	out	3V3	USB Over Current Detect Input. This pin used for overcurrent detection of USB Port #4 and/or #5.			
USB_6_7_OC#	79	out	3V3	USB Over Current Detect Input. This pin used for overcurrent detection of USB Port #6 and/or #7.			
USB_VBUS	91	out	3V3 ?	USB Client mode Power Input.			It is possible to connect 5v
USB_ID	92	out	3V3 10kΩ pull-down	USB ID Input. USB Port #1 has set to work in Host mode.			
USB_OTG_PEN	56	In	3V3	USB Power enable pin for USB Port 1.			Not used.

CAN interface signals

Signals involved with CAN interface are the following:

Q7 CAN signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
CAN0_TX	129	in	3V3	CAN Transmit Input for CAN Bus Channel 0.	
CAN0_RX	130	out	3V3	CAN Receive Output for CAN Bus Channel 0.	

SPI interface signals

Signals involved with SPI management are the following:

Q7 SPI signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
SPI_MOSI	199	in	3V3	SPI Master Out Slave In, output from Q7 module to the SPI devices.	
SPI_MISO	201	out	3V3	SPI Master In Slave Out, Input to Q7 module from SPI devices.	
SPI_SCK	203	in	3V3	SPI Clock, Output to the SPI devices from Q7 module.	
SPI_CS0#	200	in	3V3	SPI primary Chip select.	
SPI_CS1#	202	in	3V3	SPI secondary Chip select. This signal used only in case there are two SPI devices connecting to Q7_Base, and the first chip select signal (SPI_CS0#) has already been used.	

LVDS Flat Panel signals

It is available two LVDS channels, each one consisting of 1 clock pair and four data pairs.

It is possible to configure LVDS (in Q7 module) output so that it can be used as: One single channel, Two identical single channel outputs, Two independent single channel outputs.

Here following the signals related to LVDS management:

Q7 LVDS signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
LVDS_A0+	99	in		LVDS Channel #0 differential data pair #0.	eDP0_TX0+	eDP channel differential data pair #0.	
LVDS_A0-	101				eDP0_TX0-		

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
LVDS_A1+	103	in		LVDS Channel #0 differential data pair #1.	eDP0_TX1+	eDP channel differential data pair #1.	
LVDS_A1-	105				eDP0_TX1-		
LVDS_A2+	107	in		LVDS Channel #0 differential data pair #2.	eDP0_TX2+	eDP channel differential data pair #2.	
LVDS_A2-	109				eDP0_TX2-		
LVDS_A3+	113	in		LVDS Channel #0 differential data pair #3.	eDP0_TX3+	eDP channel differential data pair #3.	
LVDS_A3-	115				eDP0_TX3-		
LVDS_A_CLK+	119	in		LVDS Channel #0 differential Clock.	eDP0_AUX+	eDP channel differential auxiliary channel.	
LVDS_A_CLK-	121				eDP0_AUX-		
LVDS_B0+	100	in		LVDS Channel #1 differential data pair #0.	eDP1_TX0+	eDP secondary channel differential pair 0.	
LVDS_B0-	102				eDP1_TX0-		
LVDS_B1+	104	in		LVDS Channel #1 differential data pair #1.	eDP1_TX1+	eDP secondary channel differential pair 1.	
LVDS_B1-	106				eDP1_TX1-		
LVDS_B2+	108	in		LVDS Channel #1 differential data pair #2.	eDP1_TX2+	eDP secondary channel differential pair 2.	
LVDS_B2-	110				eDP1_TX2-		
LVDS_B3+	114	in		LVDS Channel #1 differential data pair #3.	eDP1_TX3+	eDP secondary channel differential pair 3.	
LVDS_B3-	116				eDP1_TX3-		
LVDS_B_CLK+	120	in		LVDS Channel #1 differential Clock.	eDP1_AUX+	eDP secondary auxiliary channel.	
LVDS_B_CLK-	122				eDP1_AUX-		

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
LVDS_PPEN	111	in	3V3	Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.			
LVDS_BLEN	112	in	3V3	Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.			
LVDS_BLT_CTRL/ GP_PWM_OUT0	123	in	3V3	This signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. When backlight brightness control via PWM is not required, this signal can be used as a General Purpose PWM output.			
LVDS_BLC_DAT	126	in/out	3V3	I2C control data line for external Spread Spectrum Control Clock chip.	eDP0_HPD#	eDP primary Hotplug detection.	

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
LVDS_BLC_CLK	128	in/out	3V3	I2C control clock line for external Spread Spectrum Control Clock chip.	eDP1_HPD#	eDP secondary Hotplug detection.	
LVDS_DID_DAT	125	in/out	3V3	DisplayID DDC Data line for LVDS flat Panel detection.			
LVDS_DID_CLK	127	in/out	3V3	DisplayID DDC Clock line for LVDS flat Panel detection.			

Audio interface signals

The signals related to Audio interface:

Q7 Audio signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
HDA_SYNC	59	in	3V3	Serial Bus Synchronization.	
HDA_RST#	61	in	3V3	Codec Reset.	
HDA_BCLK	63	in	3V3	Serial Bit Clock signal.	
HDA_SDO	67	in	3V3	Serial Data Out signal.	
HDA_SDI	65	out	3V3	Serial Data In signal.	

HDMI interface signals/DP interface signals

By using HDMI interface along with two LVDS single channel interfaces, it is possible to drive up to 3 independent displays.

Signals involved in HDMI management are the following:

Q7 HDMI signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
TMDS_CLK+	131	in		TMDS differential Clock.	DP_LANE3+	Display Port differential pair #3.	
TMDS_CLK-	133	in	DP_LANE3-				

Signal Name	Pin(s)	Direction	Voltage standard	Description	Alternative	Alternative Description	Comments
TMDS_TX0+	143	in		TMDS differential pair #0.	DP_LANE2+	Display Port differential pair #2.	
TMDS_TX0-	145	in	DP_LANE2-				
TMDS_TX1+	137	in		TMDS differential pair #1.	DP_LANE1+	Display Port differential pair #1.	
TMDS_TX1-	139	in	DP_LANE1-				
TMDS_TX2+	149	in		TMDS differential pair #2.	DP_LANE0+	Display Port differential pair #0.	
TMDS_TX2-	151	in	DP_LANE0-				
HDMI_CTRL_DAT	150	in/out	3V3	DDC Data line for HDMI panel.			
HDMI_CTRL_CLK	152	in/out	3V3	DDC Clock line for HDMI panel.			
HDMI_HPD#	153	out	3V3	Hot Plug Detect Output signal.			
HDMI_CEC	124	in/out	3V3	HDMI Consumer Electronics Control (CEC) Line.			
					DP_AUX+	Display Port auxiliary channel differential pair.	in/out pin 138
					DP_AUX-		in/out pin 140
					DP_HPD#	DisplayPort Hot Plug Detect output signal.	3V3 level out pin 154 not used.

LPC/GPIO interface signals

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy devices such as a Super I/O controller or a firmware hub device.

There are 8 pins that can be used for implementation of Low Pin Count (LPC) Bus interface or as General Purpose I/Os (GPIO).

When the Q7 module is programmed for LPC Interface, following signals will be available:

Q7 LPC/GPIO signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
LPC_AD[0÷3]	185-188	in/out	3V3	LPC data bus, bidirectional signal.	in/out signals GPIO0-GPIO3
LPC_CLK	189	in	3V3	LPC Clock Input line.	in/out signal GPIO4
LPC_FRAME#	190	in	3V3	LPC Frame indicator. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.	in/out signal GPIO5
LPC_LDRQ#	192	out	3V3	LPC DMA request. This signal is used only by peripherals requiring DMA or bus mastering.	in/out signals GPIO7
SERIRQ	191	in/out	3V3	LPC Serialised IRQ request, bidirectional line. This signal is used only by peripherals requiring Interrupt support.	in/out signals GPIO6

When the Q7 module is programmed for GPIOs, all previous signals are not available and corresponding pins on Qseven connector are General Purpose I/Os, bidirectional signals at +3.3V electrical level.

I2C interface signals

Signals involved with I2C interface are the following:

Q7 I2C signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
SMB_CLK	60	in/out	3V3 4k7Ω pull-up	SM Bus control clock line for System Management.	
SMB_DAT	62	in/out	3V3 4k7Ω pull-up	SM Bus control data line for System Management.	
SMB_ALERT#	64	in/out	3V3 4k7Ω pull-up	SM Bus Alert line for System Management.	
GP0_I2C_CLK	66	in/out	3V3	General purpose I2C Bus clock line.	
GP0_I2C_DAT	68	in/out	3V3	General purpose I2C Bus data line.	

Power Management signals

There is a set of signals that are used to manage the power rails and power states.

The signals involved are:

Q7 power signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
PWGIN	26	out	5V	Power Good. This signal signals that power supply section is ready and stable.	
PWRBTN#	20	out	3V3 10kΩ pull-up	Power Button. This signal connected to a push-button SW1: a pulse to GND of this signal switch power supply On or Off.	
RSTBTN#	28	out	3V3 10kΩ pull-up	Reset Button. This signal connected to a push-button SW2: a pulse to GND of this signal reset the Q7 module.	
BATLOW#	27	out	3V3 10kΩ pull-up	Battery Low.	Not used.
WAKE#	17	out	3V3 10kΩ pull-up	Wake Output.	Not used.
SUS_STAT#	19	in	3V3	Suspend status. This input connected to X14.	
SUS_S3#	18	in	3V3	S3 status input.	Not used.
SUS_S5#	16	in	3V3	S5 State input: This signal indicates S4 or S5 (Soft Off) state.	Not used.
SLP_BTN#	21	out	3V3 10kΩ pull-up	Sleep button.	Not used.
LID_BTN#	22	out	3V3 10kΩ pull-up	LID button.	Not used.

Fan Control Implementation

Q7 fan control

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
FAN_T_IN	195	out	3V3	Fan tachometer input (can be used as General Purpose Timer Input).	
FAN_OUT	196	in	3V3	Fan speed control (can be used as General Purpose PWM Output).	

Thermal Management Signals

Q7 thermal management signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
THRM#	69	out	3V3	Thermal Alarm Input to indicate an over temperature situation (can be used to initiate thermal throttling).	

THRMTRIP#	71	in	3V3	This signal used to communicate Q7_Base devices. Thermal Trip indicates an overheating condition of the processor.	

Miscellaneous signals

Q7 miscellaneous signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
WDTRIG#	70	out	3V3	Watchdog Trigger Signal.	
WDOUT	72	in	3V3	Watchdog event indicator.	
SPKR	194	in	3V3	Speaker output.	
BIOS_DIS#	41	out	3V3	Module BIOS disable input signal.	

Manufacturing signals

This pins are reserved for manufacturing and debugging purposes.

Q7 manufacturing signals

Signal Name	Pin(s)	Direction	Voltage standard	Description	Comments
MFG_NC0	207	out	3V3	JTAG_TCK / specific control signal	May be used as **JTAG_TCK** signal for boundary scan purposes during production or as a vendor specific control signal.
MFG_NC1	209	in	3V3	JTAG_TDO / UART_TX	May be used as **JTAG_TDO** signal for boundary scan purposes during production. May also be used, via a multiplexer, as a **UART_TX** signal to connect a simple UART for firmware and boot loader implementations.
MFG_NC2	208	out	3V3	JTAG_TDI / UART_RX	May be used as **JTAG_TDI** signal for boundary scan purposes during production. May also be used, via a multiplexer, as a **UART_RX** signal to connect a simple UART for firmware and boot loader implementations.
MFG_NC3	210	out	3V3	JTAG_TMS / BOOT	May be used as **JTAG_TMS** signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific **BOOT** signal for firmware and boot loader implementations.
MFG_NC4	204	out	3V3 10kΩ pull-down	JTAG-TRST / control signal for a multiplexer circuit	May be used as **JTAG_TRST#** signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). Can use 10kΩ pull-up resistor.

GND signals

Q7 GND

Pin(s)	Description	Comments
1, 2, 23, 24, 25, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197, 198	GND	Ground

Power signals

Q7 power

Signal Name	Pin(s)	Voltage standard	Description	Comments
VCC	219-230	5V	Power Supply +5V .	
VCC_5V_SB	205, 206	5V	Standby Power Supply +5V.	
VCC_RTC	193	3V	+3V Real Time Clock (RTC) supply voltage (3V backup cell input. Used for RTC operation and storage register non-volatility in the absence of system power).	

NC and reserved signals

Q7 NC and reserved signals

Signal Name	Pin(s)	Voltage standard	Description	Comments
reserved (SDIO_LED)	44		SDIO_LED	
reserved (SDIO_DAT5)	52		SDIO_DAT[4...7]	
reserved (SDIO_DAT4)	53			
reserved (SDIO_DAT7)	54			
reserved (SDIO_DAT6)	55			
NC (VCC)	211-218		These pins reserved for use in later Qseven® revisions to avoid backward compatibility issues in the future.	

SPI

The Q7_Base provides connection to the Serial Peripheral Interface (SPI) Bus via connector X13, SPI signals are connected to Q7 connector.

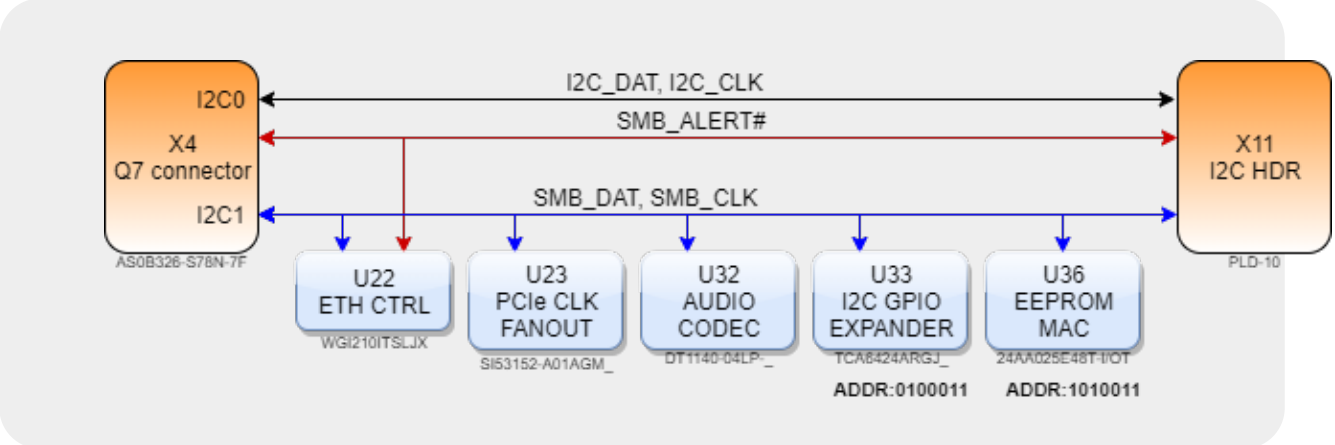
The 10 pin socket can be used for connection for external interface - SPI EEPROM and Serial Flash devices. For example, you can a 3.3V serial flash in the socket to boot the system from external BIOS.

SPI Connector

Function	SPI Connector	
Location	X13	
P/N	PLD-10	
Pinout	**Pin**	**Description**
	1	SPI_MOSI
	2	GND
	3	SPI_MISO
	4	GND
	5	SPI_SCK
	6	GND
	7	SPI_CS1
	8	GND
	9	SPI_CS0
	10	GND

I2C

Three I2C interfaces is available on Q7_Base: 2x I2C Q7_module to Q7_Base, 1x I2C MCU (STM8) Q7_Base control (see MCU).



I2C Q7Base
I2C Connector

Function	I2C Connector	
Location	X11	
P/N	PLD-10	
Pinout	Pin	Description
	1	I2C1_SMB_SCL
	2	GND
	3	I2C1_SMB_SDA
	4	GND
	5	SMB_ALERT#
	6	GND
	7	I2C0_SCL
	8	GND
	9	I2C0_SDA
	10	GND

LPC

To support LPC and GPIO devices, the LPC and GPIO signals are shared on the Q7_Base from Q7 module. The shared signals are connected to pin header X12.

This header can be used for debugging or to connect devices such as Super I/O for evaluation.

LPC/GPIO Connector

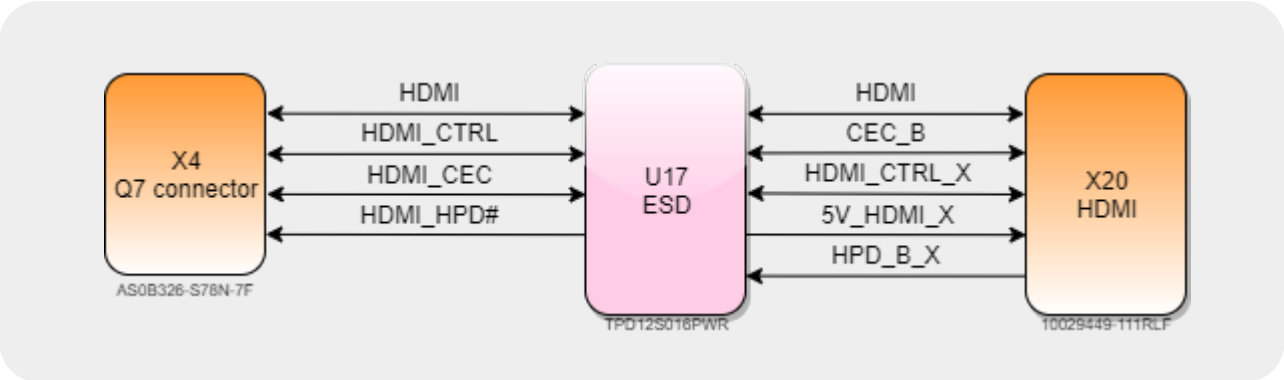
Function	LPC/GPIO Connector	
Location	X12	
P/N	PLD-10	
Pinout	Pin	Description
	1	LPC_GPIOX8_LDRQ#
	2	LPC_GPIOX8_AD1
	3	LPC_GPIOX8_AD3
	4	LPC_GPIOX8_AD0
	5	LPC_GPIOX8_FRAME#
	6	GND
	7	LPC_GPIOX8_AD2
	8	LPC_GPIOX8_CLK
	9	LPC_GPIOX8_SERIRQ
	10	GND

HDMI

HDMI signals are shared on the Q7_Base devices (using connector X20) from Q7 module (X4).

For high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) is used High Definition Multimedia Interface (HDMI) device TPD12S016 with auto-direction sensing I2C

voltage level shift buffers, with integrated protection diodes, with current limited 5-V output HDMI power line and with reverse current blocking when the system is powered off.



HDMI Q7Base
HDMI Connector

Function	HDMI Connector			
Location	X20			
P/N	10029449-111RLF Amphenol			
Pinout	**Pin**	**Description**	**Pin**	**Description**
	1	DP_D0_P (D2+)	11	GND
	2	GND	12	DP_D3_N (CLK-)
	3	DP_D0_N (D2-)	13	CEC_B_X
	4	DP_D1_P (D1+)	14	NC
	5	GND	15	HDMI_SCL_X
	6	DP_D1_N (D1-)	16	HDMI_SDA_X
	7	DP_D2_P (D0+)	17	GND
	8	GND	18	5V_HDMI_X
	9	DP_D2_N (D0-)	19	HPD_B_X
	10	DP_D3_P (CLK+)		

LVDS

This connector provides data and power connection between the Q7_Base and the Display.

The Q7_Base supports two LVDS panels can be used at the same time.
The Q7_Base has two LVDS ports, A and B, which can either be used for one panel with up to 165 Mpixel/s or as two separate ports up to 85 Mpixel/s. In either configuration, the Qseven specification only provides one set of backlight and panel power enable signals as well as one brightness control signal for both of them.

The panel can be enabled with he LVDS_PPEN signal and the backlight can be switched on with LVDS_BLEN.

One LVDS Panel

Connection one display to port A. LVDS_B signals are not used.

One LVDS Panel with a higher resolution

In this option connection LVDS_A and LVDS_B signals to the connector X19.

Two LVDS Panel

Connection two LVDS panels. Panel 1 – the primary one – is connected to port A with its corresponding panel power enable signal and the associated backlight enable signal.

This connector provides data and power connection between the Q7_Base and the Display.

LVDS Connector

Function	LVDS Connector			
Location	X19			
P/N	B34B-PHDSS_ JST Sales America Inc.			
Pinout	**Pins**	**Name**	**Pins**	**Name**
	1	LVDS_DID_SCL	18	LVDS_BLT_CTRL
	2	LVDS_DID_SDA	19	GND
	3	3V3	20	LVDS_A_D3_N
	4	3V3	21	LVDS_B_D0_P
	5	LVDS_A_D0_N	22	LVDS_B_D0_N
	6	GND	23	LVDS_B_D1_N
	7	LVDS_PPEN	24	GND
	8	LVDS_A_D0_P	25	GND
	9	LVDS_A_D1_P	26	LVDS_B_D1_P
	10	LVDS_A_D1_N	27	LVDS_B_D2_P
	11	LVDS_A_D2_P	28	LVDS_B_D2_N
	12	LVDS_BLEN	29	LVDS_B_CLK_P
	13	eDP0_HPD	30	GND
	14	LVDS_A_D2_N	31	eDP1_HPD
	15	LVDS_A_CLK_P	32	LVDS_B_CLK_N
	16	LVDS_A_CLK_N	33	LVDS_B_D3_N
	17	LVDS_A_D3_P	34	LVDS_B_D3_P

LVDS power and control

Connector X24 on Q7_Base is a 5-pin header designated for backlight voltage. Supply voltage for the backlight converter can be set to +12V or +5V.

LVDS Controls panel

Function	LVDS Controls panel	
Location	X24	
P/N	B5B-PH-K-S_	
Pinout	**Pin**	**Description**
	1	12VINT
	2	GND
	3	LVDS_BLEN
	4	LVDS_BLT_CTRL
	5	5V

Fuses F1 (12VINT) and F2 (5V) are additionally installed on the power circuit.

USB

Four USB interfaces is available on Q7_Base: 3xUSB 3.0, 1xUSB 2.0.

USB port #0, #1, #2, along with the Superspeed USB port #0, #1, #2, are carried to a standard USB 3.0 Type A receptacle.

USB port #3 are carried out to standard USB 2.0 Type A receptacles.

Debug console (USB to UART bridge) are carried out to standard USB 2.0 Type B receptacles.

For EMI/ESD protection and overcurrent protection, USB Switch, TVS and ESD Diodes are used on USB data and voltage lines.

USB Port 0

USB Port 0 Connector

Function	USB Port 0 Connector	
Location	X15	
P/N	10132411-00021LF AMPHENOL	
Pinout	**Pin**	**Description**
	1	5V0_P0 (VBUS)
	2	USB0_X_N (D-)
	3	USB0_X_P (D+)
	4	GND
	5	USB6_SSRX0_N (STDA_SSRX-)
	6	USB6_SSRX0_P (STDA_SSRX+)
	7	GND
	8	USB7_SSTX0_N (STDA_SSTX-)
	9	USB7_SSTX0_P (STDA_SSTX+)

USB Port 1

USB Port 1 Connector

Function	USB Port 1 Connector	
Location	X16	
P/N	10132411-00021LF AMPHENOL	
Pinout	**Pin**	**Description**
	1	5V0_P1 (VBUS)
	2	USB2_X_N (D-)
	3	USB2_X_P (D+)
	4	GND
	5	USB4_SSRX2_N (STDA_SSRX-)
	6	USB4_SSRX2_P (STDA_SSRX+)
	7	GND
	8	USB5_SSTX2_N (STDA_SSTX-)
	9	USB5_SSTX2_P (STDA_SSTX+)

USB Port 2

USB Port 2 Connector

Function	USB Port 2 Connector	
Location	X17	
P/N	10132411-00021LF AMPHENOL	
Pinout	**Pin**	**Description**
	1	5V0_P2 (VBUS)
	2	USB1_X_N (D-)
	3	USB1_X_P (D+)
	4	GND
	5	USB_SSRX1_N (STDA_SSRX-)
	6	USB_SSRX1_P (STDA_SSRX+)
	7	GND
	8	USB_SSTX1_N (STDA_SSTX-)
	9	USB_SSTX1_P (STDA_SSTX+)

USB Port 3

USB Host 3 signals from the Q7 connector is connected to standard USB Type-A connector.

USB Port 3 Connector

Function	USB Port 3 Connector	
Location	X18	
P/N	292303-1 TECONN	
Pinout	**Pin**	**Description**
	1	5V0_P3 (VCC)
	2	USB3_X_N (DM)
	3	USB3_X_P (DP)
	4	G
	G	GND

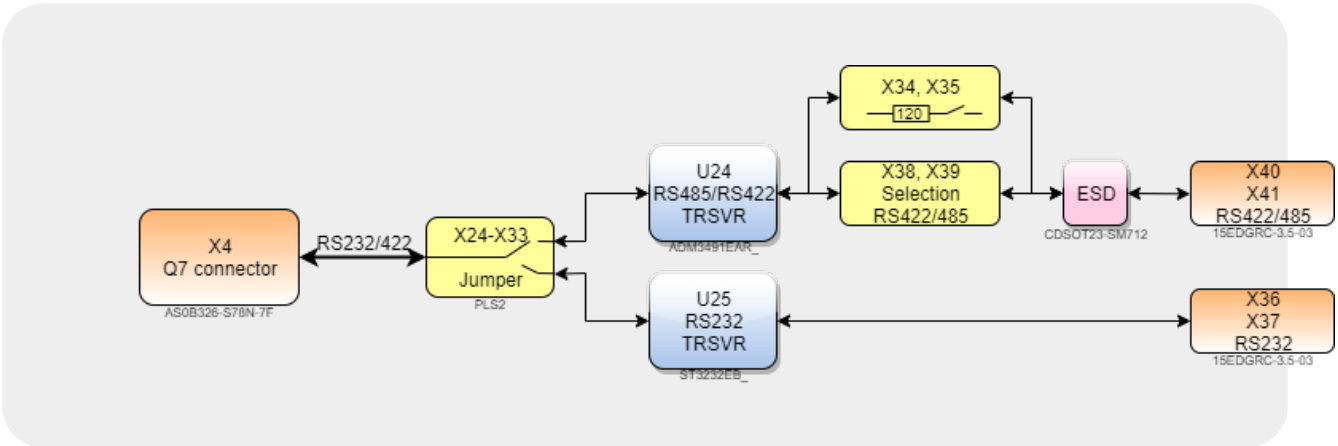
Debug console (USB to UART bridge)

For converting UART to USB used a USB-to-Dual-UART Bridge Controller CP2105 (U2). The CP2105 includes a USB 2.0 fullspeed function controller, USB transceiver, oscillator, one-time programmable ROM, and two asynchronous serial data buses (UART) with full modem control signals.
For asynchronous communication between two data buses is used dual-bit noninverting bus transceiver with two separate configurable power-supply rails the SN74AVC (U3).

Q7Base USB debug console
USB Connector (USB to UART console)

Function	USB (USB to UART console) Connector	
Location	X8	
P/N	1734035-1 TECONN	
Pinout	**Pin**	**Description**
	1	VCC
	2	DM
	3	DP
	4	ID
	5	GND

Serial



Q7Base serial diagram

For connection to standard serial ports (like those offered by common PCs, for example) it is include RS-232 transceiver ST3232EB_ (U25) and RS-485 transceiver ADM3491EAR_ (U24) on

the board.

Jumpers for RS-232\RS485\RS422 selection

Jumpers for RS-232\RS485\RS422 selection

	X24	X25	X26	X27	X28	X29	X30	X31	X32	X33	X38	X39
RS232	-	+	-	+	-	+	-	+	-	+	-	-
RS422	+	-	+	-	+	-	+	-	+	-	-	-
RS485	+	-	+	-	+	-	+	-	+	-	+	+

where “+“ means Populated, “- “ - Not Populated

RS-232

RS232 Data Connection

Function	RS232 Data Connection	
Location	X36	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	RX
	2	TX
	3	GND

RS232 detect Connection

Function	RS232 detect Connection	
Location	X37	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	CTS
	2	RTS
	3	GND

RS-485\RS-422

Jumpers for RS-485\RS422 selection and options

Optional jumpers - Using termination resistors

To suppress reflection at the end of the line, it is recommended to add termination resistors between signal pairs at both ends of the cable.
The Q7_Base have on board termination resistors that can be enabled through jumpers, so if a device is placed at one of the ends of the cable place jumpers on required position.

Optional jumpers - Using termination resistors

	X34	**X35**
Adding termination resistors to the line	Populated	Populated
No termination resistors to the line	Not Populated	Not Populated

When adding termination to the line, no more than two resistors should be used, one at each end of the line.

Optional jumper - Selection control method for receiver and driver

Optional jumper-for Selection control method for receiver and driver

X49	**RS422/RS485 mode**
Populated	Using external signal DE to control Driver/Receiver ADM3491 on Q7_Base.
Not Populated	Using external signal DE to control Driver ADM3491 and signal RE_N to control Receiver ADM3491 on Q7_Base.

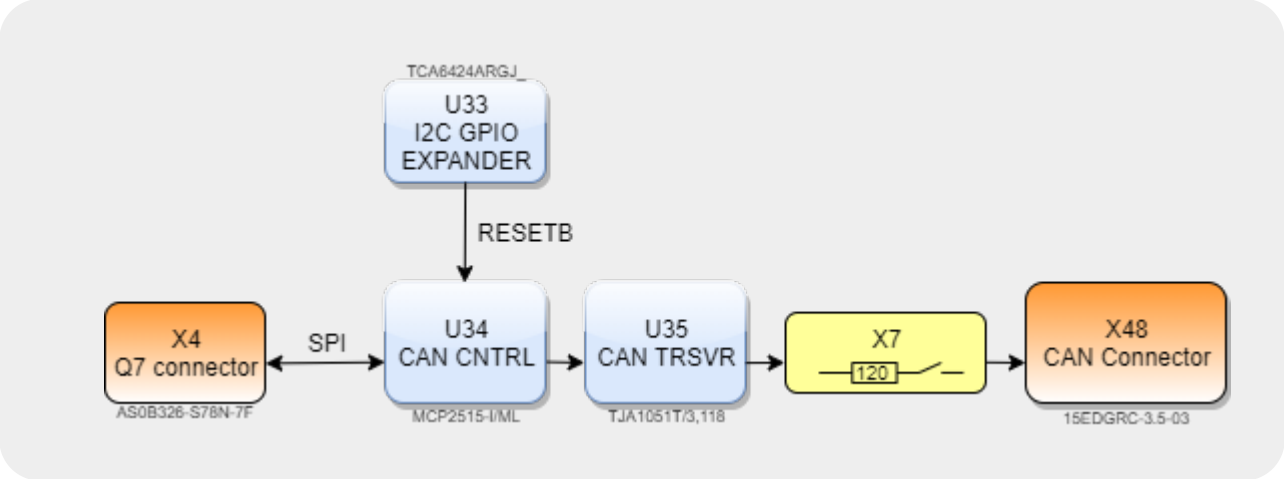
RS485 data1 Connection

Function	RS485 data1 Connection	
Location	X40	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	A
	2	B
	3	GND

RS485 data2 Connection

Function	RS485 data2 Connection	
Location	X41	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	Z
	2	Y
	3	GND

CAN



Q7Base CAN diagram

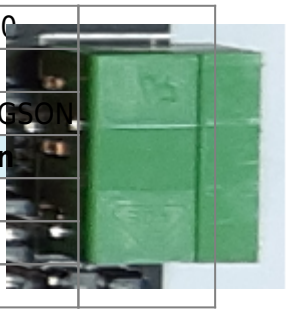
CAN port 0

To connect Qseven CAN interface (Q7 module) to CAN Bus on Q7_Base, it is integrate a

CAN Bus Transceiver TJA1051T/3,118 (NXP) on the board.

CAN Connector port 0

Function	CAN Connector port 0	
Location	X23	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	CANH_0
	2	GND
	3	CANL_0



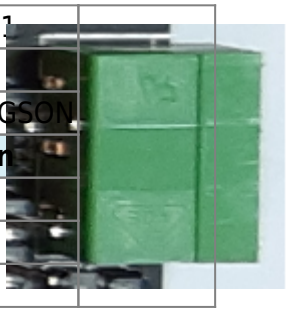
CAN Bus connection is made through a pluggable terminal block (15EDGRC-3.5-03 Degson). 120Ω resistor is placed for line termination, in case that the system is placed to one of the two extremities of CAN Line. Jumper X22 enables or disables CAN bus termination.

CAN port 1

To connect Qseven module to CAN Bus on Q7_Base, it is integrate a CAN Controller MCP2515-I/ML (MICROCHIP) (use SPI interface) and Bus Transceiver TJA1051T/3,118 (NXP) on the board.

CAN Connector port 1

Function	CAN Connector port 1	
Location	X48	
P/N	15EDGRC-3.5-03 DEGSON	
Pinout	**Pin**	**Description**
	1	CANH_1
	2	GND
	3	CANL_1



CAN Bus connection is made through a pluggable terminal block (15EDGRC-3.5-03 Degson). 120Ω resistor is placed for line termination, in case that the system is placed to one of the two extremities of CAN Line. Jumper X7 enables or disables CAN bus termination.

Jumper for options

CAN optional jumper

Jumper Position	**Configuration**
Populated	There are no more devices on the line. Used terminating resistor 120Ω at the end of the bus.
Not populated	There are other devices or terminating resistor on the line.

Jumper for options

Optional jumper-CAN terminating resistor

Jumper Position	**Configuration**

Populated	There are no more devices on the line. Used terminating resistor 120Ω at the end of the bus.
Not populated	There are other devices or terminating resistor on the line.

Audio

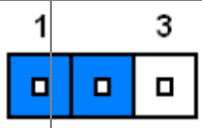
Q7_Base provides one Inter-IC Sound(I2S) interface, through audio CODEC IC SGTL5000 with I2S interface.

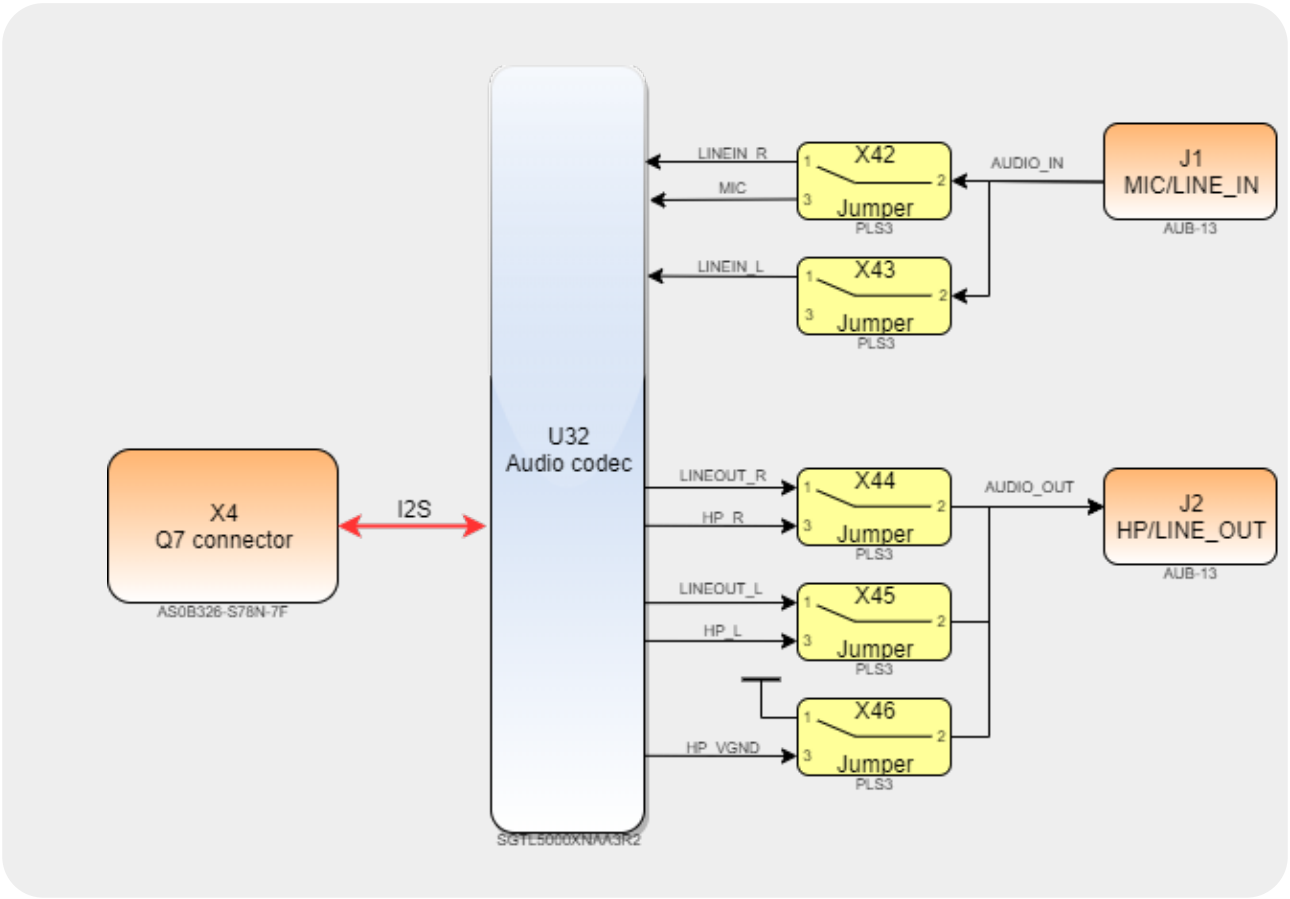
From the codec, 1 microphone input or Line in (MP3/FM) Input, 1 headphone output or Line out (Speaker Amp/Docking Station/FMTX) are available.

The board provides two jack audio connectors for input and output.

5 jumpers are used to switch alternative inputs and outputs.

3 position jumpers view

Position	Jumpers view
1-2	
2-3	



Q7Base audio diagram

Jumpers for Line selection and options

Jumpers for Line selection and options

Jumpers	LINE_IN	MIC
X42	1-2	2-3
X43	1-2	2-3

Jumpers	LINE_OUT	HP
X44	1-2	2-3
X45	1-2	2-3
X46	1-2	2-3

Ethernet

The Q7_Base is equipped with a RJ45 connector with integrated magnetics to support Gigabit Ethernet on the X9, X10 connectors. Additionally, LED indicators are integrated within the LAN connectors.

Ethernet port 1

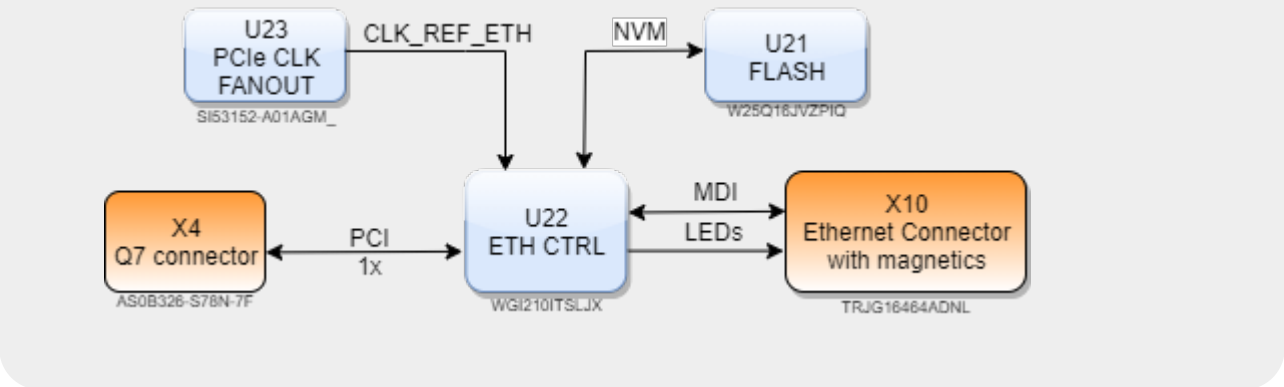
Ethernet port 1

Function	Gigabit Ethernet Connector	
Location	X9	
P/N	TRJG16464ADNL TRXCOM	
Pinout	Pin	Description
	1	GBE0_MDI0_P
	2	GBE0_MDI0_N
	3	GBE0_MDI1_P
	4	GBE0_MDI2_P
	5	GBE0_MDI2_N
	6	GBE0_MDI1_N
	7	GBE0_MDI3_P
	8	GBE0_MDI3_N

Ethernet led

Action	Description
LED 1 Yellow lit	Ethernet controller 0 link indicator, directly connected to the Q7 module.
LED 2 Green lit	Ethernet controller 0 activity indicator, directly connected to the Q7 module.

Ethernet port 2



Q7Base ethernet diagram

The PCIe v2.1 (2.5GT/s) Interface is used by the WGI210ITSLJX as a host interface. The interface only supports the PCIe v2.1 (2.5GT/s) rate and is configured to x1. For communication between Controller on Q7 module and the WGI210 used SMBus interface (see paragraph I2C for more details).

The WGI210 use an external SPI serial interface to a Flash W25Q16JVZPIQ (U21) for storing product configuration information and a boot ROM device.

The WGI210 uses a 100 MHz differential reference clock. This signal is generated on U23 (SI53152-A01AGM_) and routed to U22 (WGI210ITSLJX) .

The WGI210 implements three output drivers used for driving external LED circuits on X10 connector.

Ethernet port 2

Function	Gigabit Ethernet Conn	
Location	X10	
P/N	TRJG16464ADNL TRXCOM	
Pinout	**Pin**	**Description**
	1	GBE1_MDI0_P
	2	GBE1_MDI0_N
	3	GBE0_MDI1_P
	4	GBE1_MDI2_P
	5	GBE1_MDI2_N
	6	GBE1_MDI1_N
	7	GBE1_MDI3_P
	8	GBE1_MDI3_N

M.2 PCIe

The Q_Base is equipped with a PCI Express Mini Card socket, connector provide the ability to insert different removable PCI Express Mini Cards. The PCI Express Mini Card utilizes PCI Express link 0.

PCIE Slot

Function	PCIE Slot			
Location	X1			
P/N	MDT420M02001 AMPHENOL			
Pinout	**Pin**	**Description**	**Pin**	**Description**
	1	GND	36	NC
	2	3V3_SSD_SATA	37	NC
	3	GND	38	DEV_SLEEP_DATA
	4	3V3_SSD_SATA	39	GND
	5	NC	40	NC
	6	NC	41	SATA_B_P
	7	NC	42	NC
	8	NC	43	SATA_B_N
	9	GND	44	NC
	10	M2_LED_SATA	45	GND
	11	NC	46	NC
	12	3V3_SSD_SATA	47	SATA_A_N
	13	NC	48	NC
	14	3V3_SSD_SATA	49	SATA_A_P
	15	GND	50	NC
	16	3V3_SSD_SATA	51	GND
	17	NC	52	NC
	18	3V3_SSD_SATA	53	NC
	19	NC	54	NC
	20	NC	55	NC
	21	GND	56	NC
	22	NC	57	GND
	23	NC	58	NC
	24	NC	67	NC
	25	NC	68	NC
	26	NC	69	PEDET_SATA
	27	GND	70	3V3_SSD_SATA
	28	NC	71	GND
	29	NC	72	3V3_SSD_SATA
	30	NC	73	GND
	31	NC	74	3V3_SSD_SATA
	32	NC	75	GND
	33	GND	76	S (GND)
	34	NC	77	S (GND)
	35	NC		

M.2 SATA

SATA Slot

Function	SATA Slot			
Location	X2			
P/N	MDT420M02001 AMPHENOL			
Pinout	**Pin**	**Description**	**Pin**	**Description**
	1	GND	36	NC
	2	3V3_SSD_PCIE	37	NC
	3	GND	38	DEV_SLEEP_PCIE
	4	3V3_SSD_PCIE	39	GND
	5	NC	40	NC
	6	NC	41	SATA_B_P
	7	NC	42	NC
	8	NC	43	SATA_B_N
	9	GND	44	NC
	10	M2_LED_PCIE	45	GND
	11	NC	46	NC
	12	3V3_SSD_PCIE	47	SATA_A_N
	13	NC	48	NC
	14	3V3_SSD_PCIE	49	SATA_A_P
	15	GND	50	PERST#
	16	3V3_SSD_PCIE	51	GND
	17	NC	52	NC
	18	3V3_SSD_PCIE	53	NC
	19	NC	54	NC
	20	NC	55	NC
	21	GND	56	NC
	22	NC	57	GND
	23	NC	58	NC
	24	NC	67	NC
	25	NC	68	NC
	26	NC	69	PEDET_PCIE
	27	GND	70	3V3_SSD_PCIE
	28	NC	71	GND
	29	NC	72	3V3_SSD_PCIE
	30	NC	73	GND
	31	NC	74	3V3_SSD_PCIE
	32	NC	75	GND
	33	GND	76	S (GND)
	34	NC	77	S (GND)
	35	NC		

SD Card

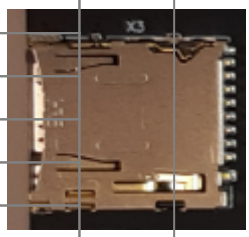
The Q7_Base provides one SD/MMC socket (X3).

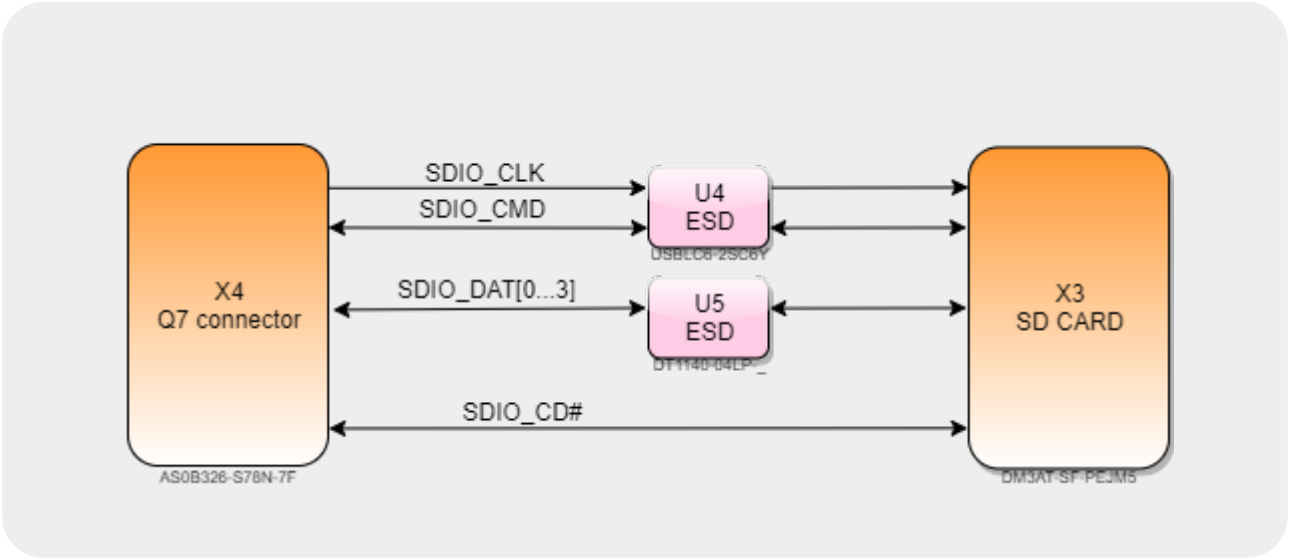
The SD Card slot can be configured as SD or MMC card operation. The SD Card Slot can

support SDIO cards designed to fit in a standard SD card slot. The main power for the Card Socket is 3.3V.

SD Card Socket

Function	SD Card Socket	
Location	X3	
P/N	DM3AT-SF-PEJM5 HIROSE	
Pinout	**Pin**	**Description**
	1	DAT2
	2	CD/DAT3
	3	CMD
	4	VDD
	5	CLK
	6	VSS
	7	DAT0
	8	DAT1
	9	CD_A
	10	CD_B





Q7Base sdio diagram

Feature Connector

Feature Connector

Function	Feature Connector	
Location	X14	
P/N	DM3AT-SF-PEJM5 HIROSE	
Pinout	Pin	Description
	1	3V3
	2	GND
	3	FAN_T_IN
	4	GND
	5	GPO0(SUS_STAT#)
	6	GND
	7	FAN_OUT/GP_PWM_OUT1
	8	GND
	9	SPKR/GP_PWM_OUT2
	10	GND

Fan Connector

The Q7_Base provides the ability to connect 3.3V cooling fans for the CPU module and system. Connector X14 is for 4pin fan. The FAN_TACHOIN signal originates from the Q7 module.

Debugging/development connectors

Connectors are provided for debugging/development purpose.

JTAG/UART

Q7_Base provides a USB Connector (UART) and JTAG connector for debugging. Both debug interfaces are sharing same signals from Q7 connector, since MFG_NCN4_MUX select line is used to select either UART or JTAG.
Q7_Base provided jumper X25 to select Debug ports. In default jumper will be on UART. A 10-pin JTAG connector is provided on the Q7_Base.

JTAG Connector

Function	JTAG			
Location	X7			
P/N	PLD-10			
Pinout	Pin	Description	Pin	Description
	1	JTAG_TCK	6	NC
	2	GND	7	NC
	3	JTAG_TDO/UART_TX	8	NC
	4	3V3	9	JTAG_TDI/UART_RX
	5	JTAG_TMS/BOOT	10	GND

UART will be used for Debug purpose. This is not the full functional UART and supports only Serial TX and RX signals.

X25 (JTAG/UART selector)

JTAG/UART selection jumper

Jumper Position	Configuration
Populated	Selecting UART for debugging.
Not populated	Selecting JTAG for debugging.

MCU programming

Connector X21 allows a debugging or programming tool to be connected to the MCU STM8 (U18).

Program/debug MCU connector

Function	Program/debug MCU	
Location	X21	
P/N	WF-4 TAB	
Pinout	Pin	Description
	1	3V3_WD
	2	SWIM
	3	GND
	4	NRST

Jumpers and Buttons

Jumpers

You can configure board to match the needs of your application by setting jumpers.

Q7Base jumpers view

X6 (Module/Carrier BIOS selector)

This signal used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.

Module/Carrier BIOS selector

Jumper Position	Configuration
Populated	Disabling the integrated Bios module on Q7 module (BIOS from Q7_Base).
Not populated	Enabling the integrated Bios module on Q7 module (BIOS from CPU Q7 Module Q7).

Buttons

Power Button SW1

The Q7_Base performs a power up sequence when you press this button. The power

button is connected to the Q7 module's PWRBTN# signal.

Reset Button SW2

When you press this button, the Q7 module and all components connected on board will perform a hard reset. The reset button is connected to the Q7 module's RSTBTN# signal.

On-board Devices

3V_battery

The recharge lithium smd battery supplies power to the RTC and memory of the Q7 module. The battery provide 3V of power. It is possible to disconnect battery by unsoldering the resistor R100 (0 Ohm).

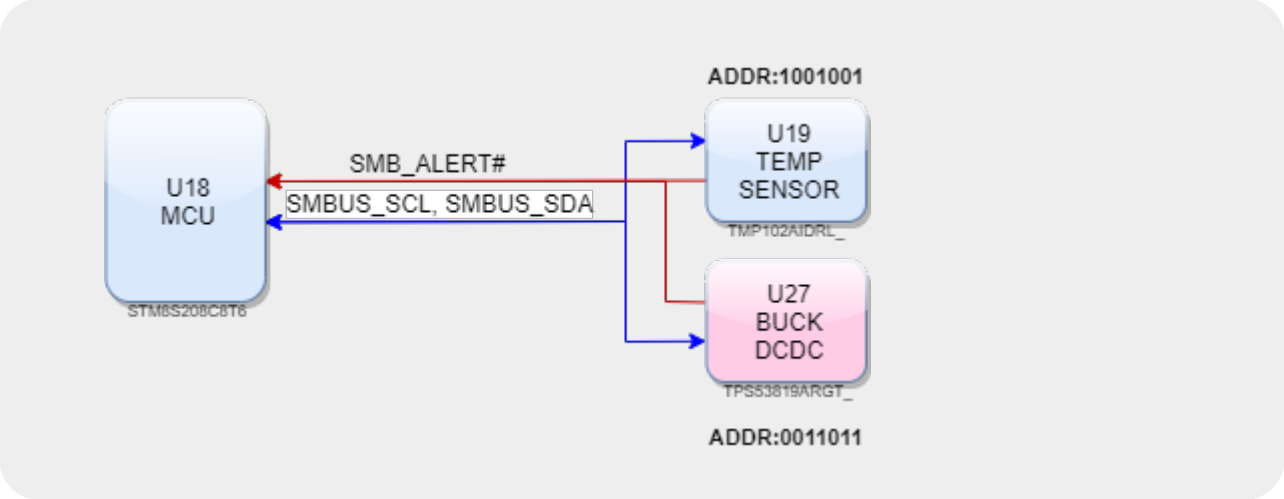
3V_battery

Function	Power VRTC	
Location	B1	
P/N	ML-1220/F1AN PANASONIC	
Pinout	**Pin**	**Description**
	1	GND
	2	BAT_OUT

MCU

The 8-bit microcontroller STM8S (U18) with 64 Kbytes Flash program memory is designed for detect the occurrence of fault, generated by external interference and used to resolve processor malfunctions due to hardware or software failures (watchdog).

The microcontroller uses the I2C bus to communicate the temperature sensor TMP102 (U19) and DCDC TPS53819 (U27).



Q7Base MCU connections

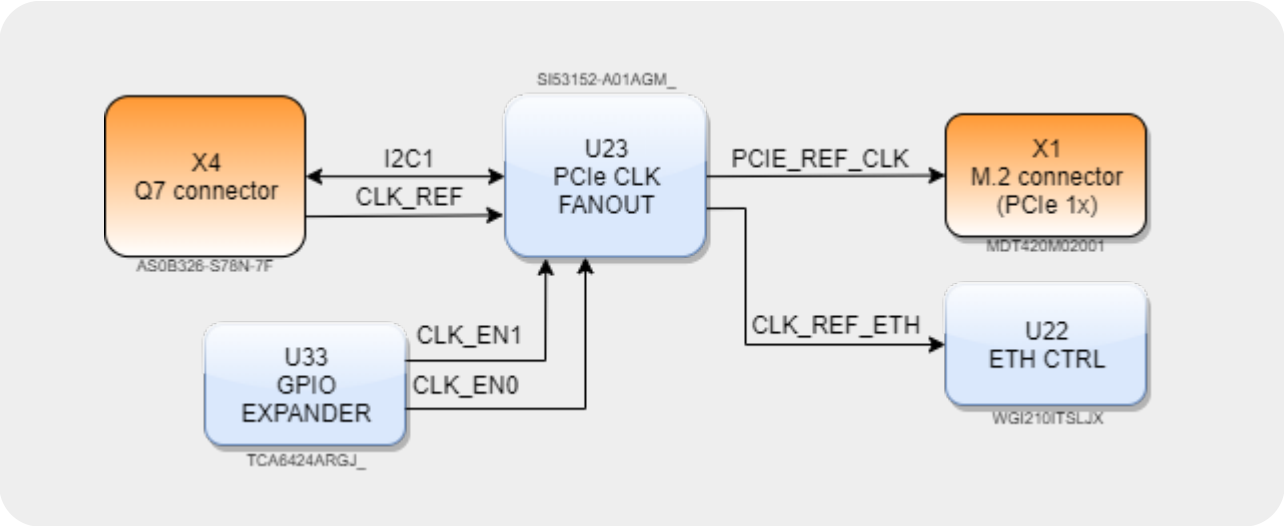
The single wire interface module (SWIM) permits non-intrusive, real-time incircuit debugging and fast memory programming.

Temperature Sensor

The TMP102 (U19) is a digital temperature sensor with SMBus alert function from Texas Instruments. TMP102 uses the I2C bus to communicate the temperature on STM8 (U18) and runs from 3.3V. The TMP102 is capable of reading temperatures to a resolution of 0.0625°C (on-chip 12-bit ADC), and is accurate up to 0.5°C.
The default address is 0x49 (1001001).

PCIe clock buffer

The Si53152 (U23) is a spread spectrum tolerant PCIe clock buffer that source two PCIe (CLK0 and CLK1) clocks simultaneously. The device has two hardware output enable inputs (CLK_EN0, CLK_EN1) for enabling the respective differential outputs on the fly. The device also features output enable control through I2C communication (Q7 module).



Q7Base PCIe clock buffer

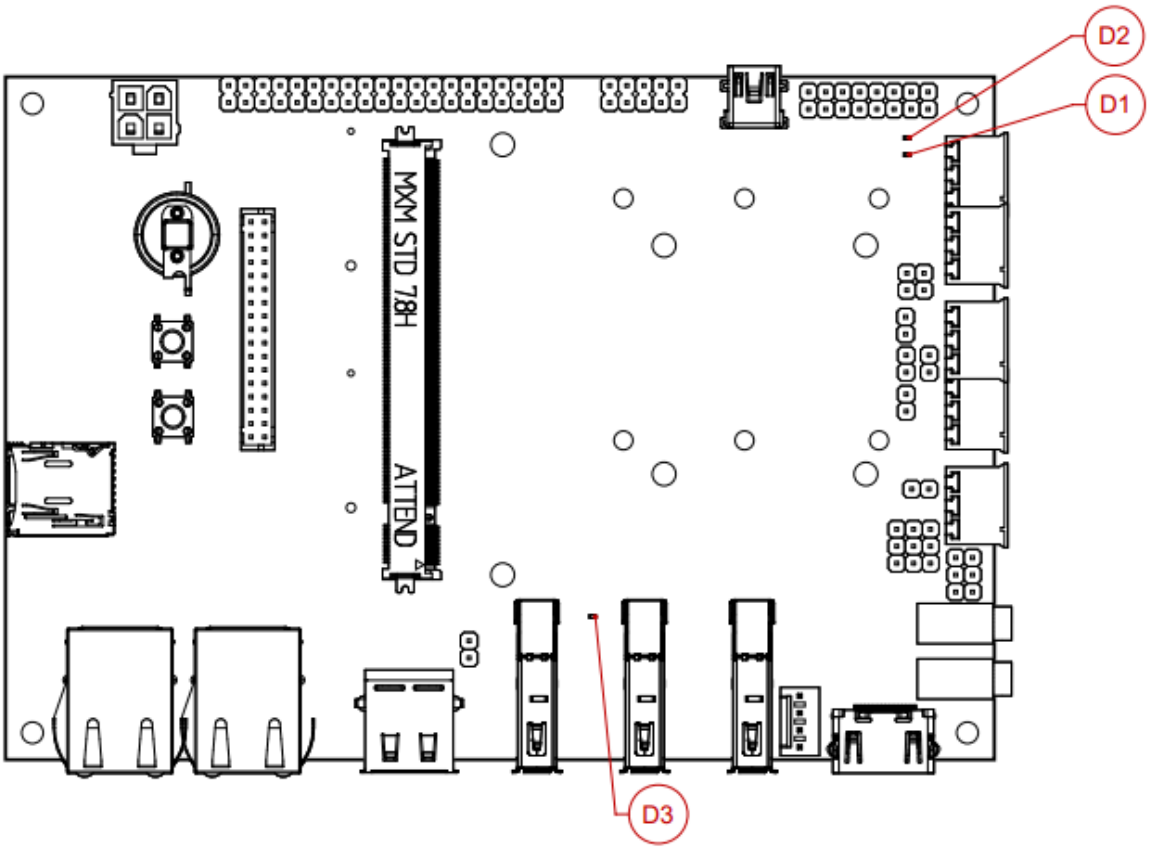
GPIO expander

TCA6424A (U33) is 24-bit I/O expander for the two-line bidirectional bus (I2C) is designed to provide remote I/O expansion via the I2C interface.
The default address is 0100011.

Status Information

LEDs

There are three green LEDs D1-D3 (LNJ347W83RA PANASONIC) on the Q7_Base.



Q7Base led view

D1

This is programmable MCU user LED.

D2

Led D2 indicates that all power rails located on the board are ready for use.

D3

User led D3 connects to custom signal and used as GPIO.