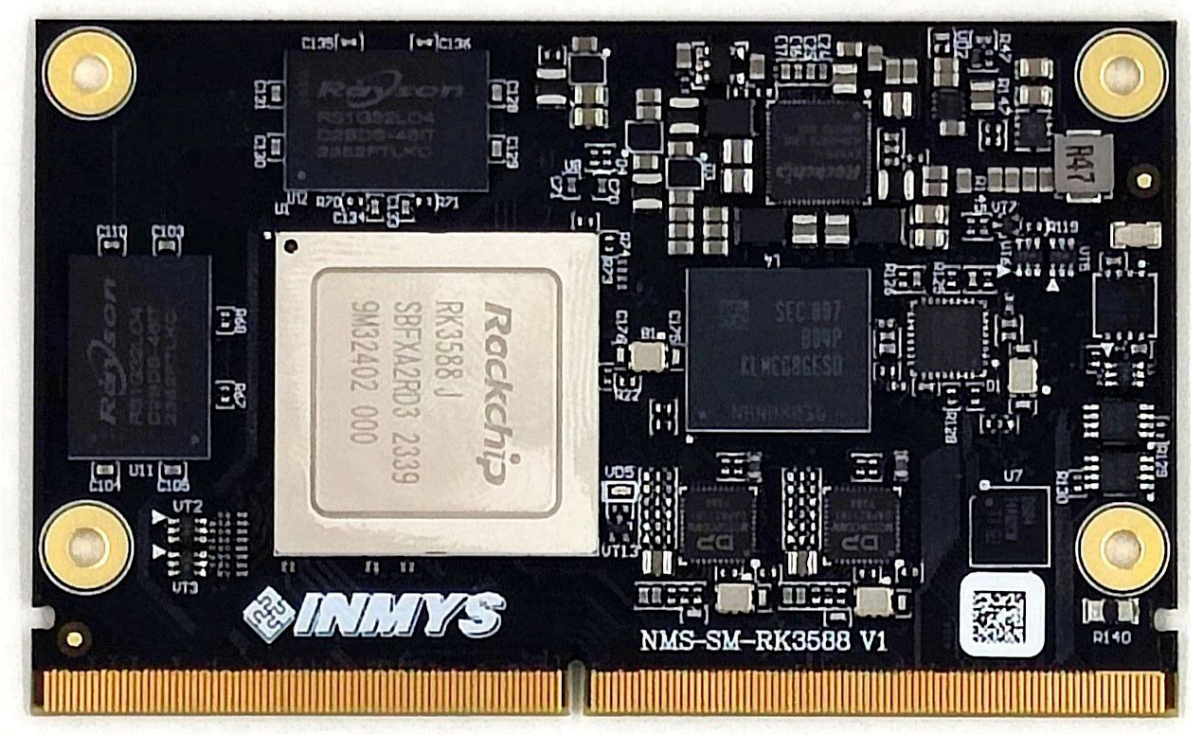
Содержание

NMS-SM-RK3588 v1 ds-ru 3
Краткое описание возможностей 4
Файлы для загрузки 5
Структурная схема модуля 6
Механические характеристики 7
Основные аппаратные компоненты 8
Расположение компонентов на плате 8
Вид сверху 8
Вид снизу 10
Процессор 10
Расположение разъемов на плате 12
Вид сверху 12
Вид снизу 13
Распиновка разъемов 13
Информация для заказа 25

NMS-SM-RK3588 v1 ds-ru



Процессорный модуль **NMS-SM-RK3588** выполнен на основе восьмиядерного процессора RK3568 производства **Rockchip**, который сочетает в себе четыре высокопроизводительных ядра Cortex-A76, четыре энергоэффективных ядра Cortex-A55, высокопроизводительный NPU и поддержку декодирования видео 8K, благодаря чему обеспечивается высокая вычислительная мощность и оптимальная производительность для многозадачных операций.

Процессорный модуль совместно с основной платой может формировать полноценную высокопроизводительную материнскую плату для промышленного применения и напрямую применяться к различным интеллектуальным продуктам, ускоряя продвижение продукта.

Модуль создан на доступной несанкционной компонентной базе и позволяет стабильно и регулярно выпускать промышленные партии изделий.

Краткое описание возможностей

Таблица 1: Основные технические характеристики

Внешние разъемы	Краевой разъём в соответствии со SMARC, по стандарту (2.0\2.1)
Процессор	RK3588J
	Ядра:4x ядра Cortex-A76 с частотой до 2,4 ГГц и 4x ядра Cortex-A55 с частотой 1,8 ГГц в конфигурации DynamIQ
	Графический ускоритель: Arm Mali-G610 MP4 «Odin» с поддержкой OpenGLES 1.1, 2.0 и 3.2, OpenCL до 2.2 и Vulkan1.2, 2D-графический механизм до 8192 × 8192 источника, 4096 × 4096 назначения
	Видеоускоритель: 8Kp60 H.265, VP9, AVS2, 8Kp30 H.264 AVC / MVC, 4Kp60 AV1, 1080p60 MPEG-2 / -1, VC-1, VP8, кодирование 8Kp30 в реальном времени с H.265 / H.264; поддерживается многоканальное кодирование при более низких разрешениях
	Нейросопроцессор: 6 TOPS NPU 3.0 (Neural Processing Unit). Поддержка INT8/16, FP16/BFP16. Поддержка фреймворков: TensorFlow, Pytorch, Caffe, ONNX, MXNet, Keras, Darknet
ОЗУ	Память: 2 канала LPDDR4x-4267 x 32, 4/8/16/32 ГБайт суммарного объема
Флэш-память	Поддержка eMMC 5.1/5.0/4.51, режимы HS400, HS200, DDR50. Объем 16ГБ/32ГБ/64ГБ и более
ЭСППЗУ	2 Кбита, доступ по I2C, уникальный идентификатор 48 бит (24AA025)
ИС управления питанием	PMIC (RK806-1)
Прочие компоненты	Часы реального времени RTC (PCF8523TK)
	2x Гигабит ETH PHY (DAP8211RI)
	MIPIDSIto2LVDS (SN65DSI84ZQER)
	PCIe Gen 4 Clock Generator (PI6CG184Q2)
	Датчик измерения тока потребления модуля (NCS211RSQT2G)
	I2C-GPIO расширитель (TPT29555-TS5R)

Интерфейсы	2x USB 2.0 Host
	2x USB 2.0/3.0 OTG
	PCIe 3.0 (конфигурация 1 x 4, 2 x 2 или 4 x 1)
	2x CAN
	4x UART (SER0 и SER2 4-х проводные (Rx, Tx, RTS, CTS), SER1 и SER3 двухпроводные (Rx, Tx))
	2x SPI
	4x I2C
	1x I2S
	2x PWM
	1x SATA
	1x HDMI
	1x DP
	2x LVDS (MIPI DSI→ 2LVDS BRIDGE)
	1x CSI0 2 lanes
	1x CSI1 4 lanes
	1x SDIO
	2x ETH 1GB (ETH PHY)
	13x GPIO
Напряжение питания	+5 Вольт
Потребление	**TBD**
Габаритные размеры	82×50 мм

Файлы для загрузки

Таблица 2: Файлы для загрузки

Название документа	Краткое описание	Версия	Дата
nms-sm-evm_v1_prod_sch.pdf	Схема электрическая принципиальная отладочной платы SMARC: NMS-SM-EVM v1	v1	2022.09.15
nms_sm_rk3588_v1_prod.step	STEP-файл модуля NMS-SM-RK3588 v1	v1	2024.06.21

Структурная схема модуля

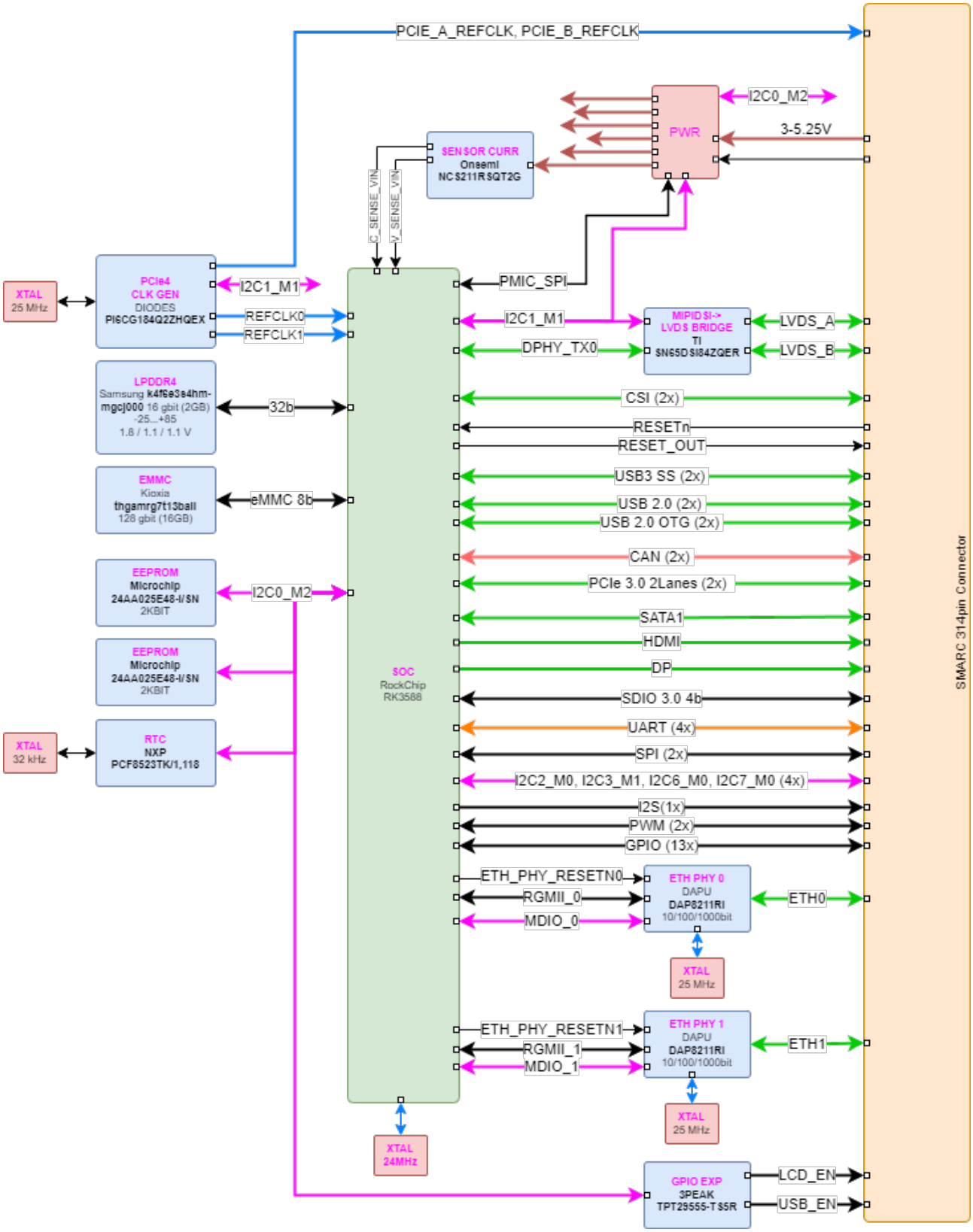


Рисунок 1: Структурная схема модуля

Механические характеристики

Размер платы : 82 x 50 мм.

Печатная плата состоит из 12 слоев, часть из которых являются заземляющими для подавления помех.

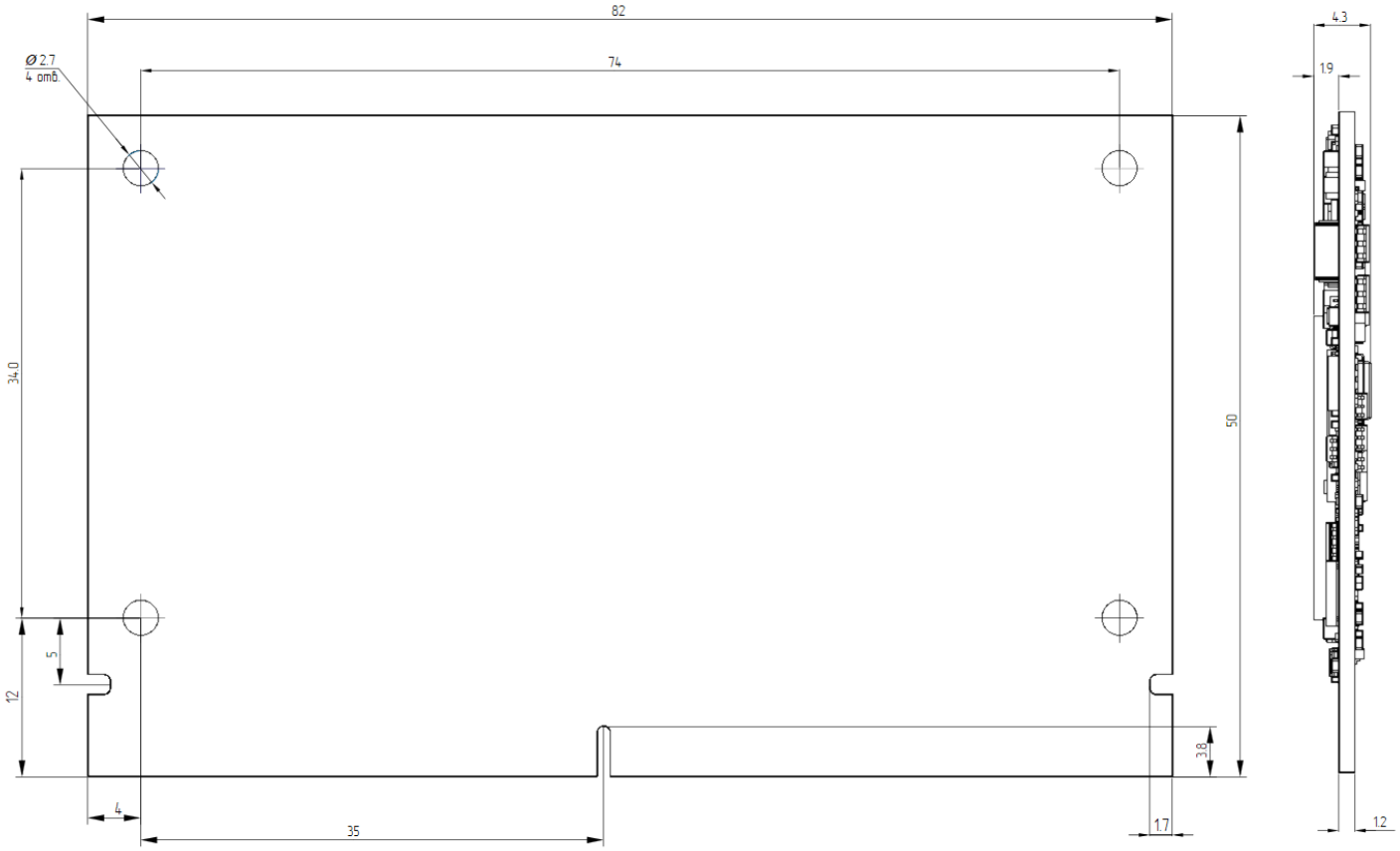


Рисунок 2: Габаритные размеры

Основные аппаратные компоненты

Расположение компонентов на плате

Вид сверху

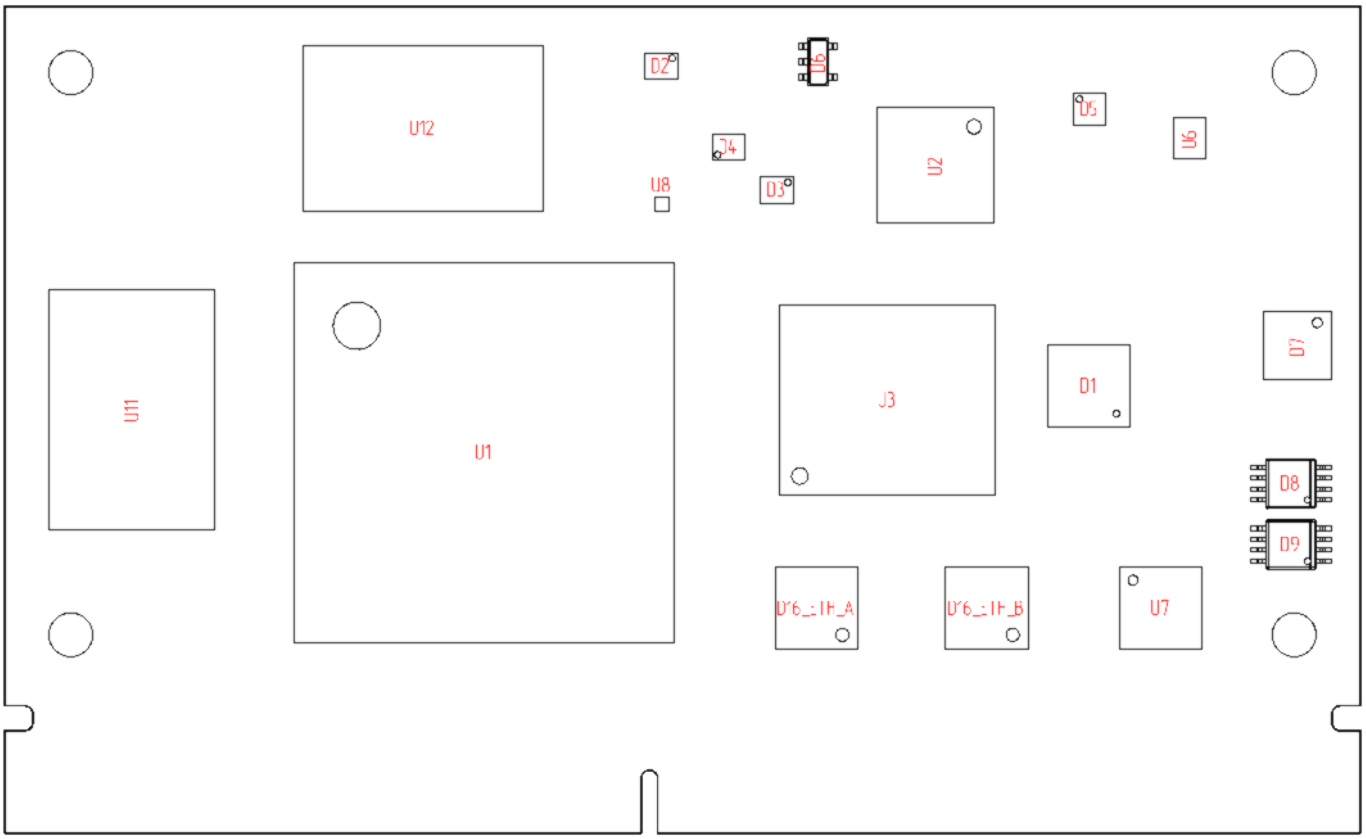


Рисунок 3: Расположение компонентов на плате. Вид сверху

Таблица 3: Наименование компонентов на плате на верхней стороне

Позиционное обозначение	P/N	Описание
D1	PI6CG184Q2ZHQEX	PCIe CLK GEN
D2, D4	RK860-2	DCDC 6A
D3	RK860-3	DCDC 7A
D5	RT5753AHGQWA	DCDC 4A
D6	SGM2576YN5G	POW SW
D7	PCF8523TK/1,118	RTC
D8, D9	RS2T45XM	LOGIC BUF
D16_ETH_A, D16_ETH_B	DAP8211RI	ETH PHY 1G
U1	RK3588	CPU
U2	RK806-1	PMIC
U3	THGAMRG7T13BAIL*	EMMC
U6	RT5789AGQUF	DCDC 6A
U7	SN65DSI84ZQER	MIPIDSIto2LVDS BRIDGE
U8	SGM2578AADYG_TR	POW SW
U11, U12	K4F6E3S4HM-MGCJ000*	LPDDR4

* - партномера микросхем памяти могут меняться в зависимости от конфигурации модуля и номера партии.

Вид снизу

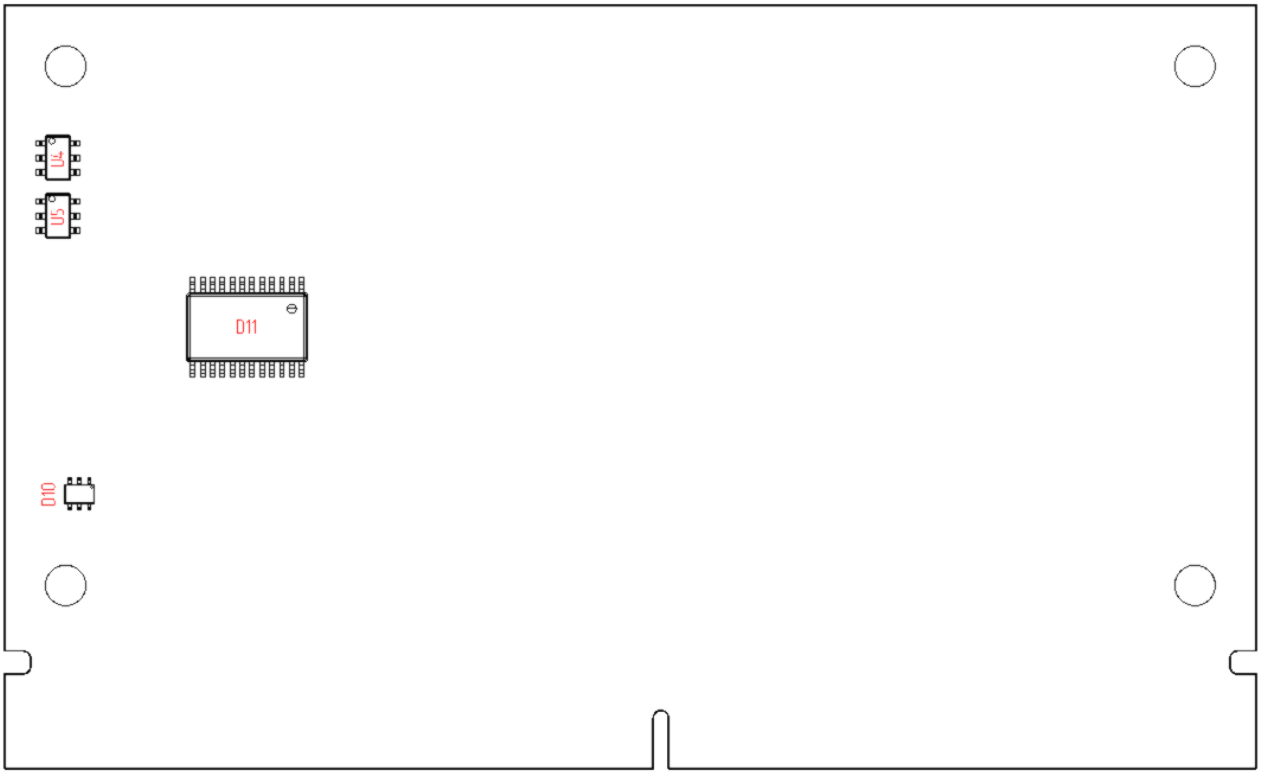


Рисунок 4: Расположение компонентов на плате. Вид снизу

Таблица 4: Наименование компонентов на плате на нижней стороне

Позиционное обозначение	P/N	Описание
U4, U5	24AA025E48T-I/OT	EEPROM 2KBIT
D10	NCS211RSQT2G	CURR SENS
D11	TPT29555-TS5R	16-bit GPIO EXPANDER

Процессор

На рисунке 5 показаны функциональные модули в процессорной системе RK3568.

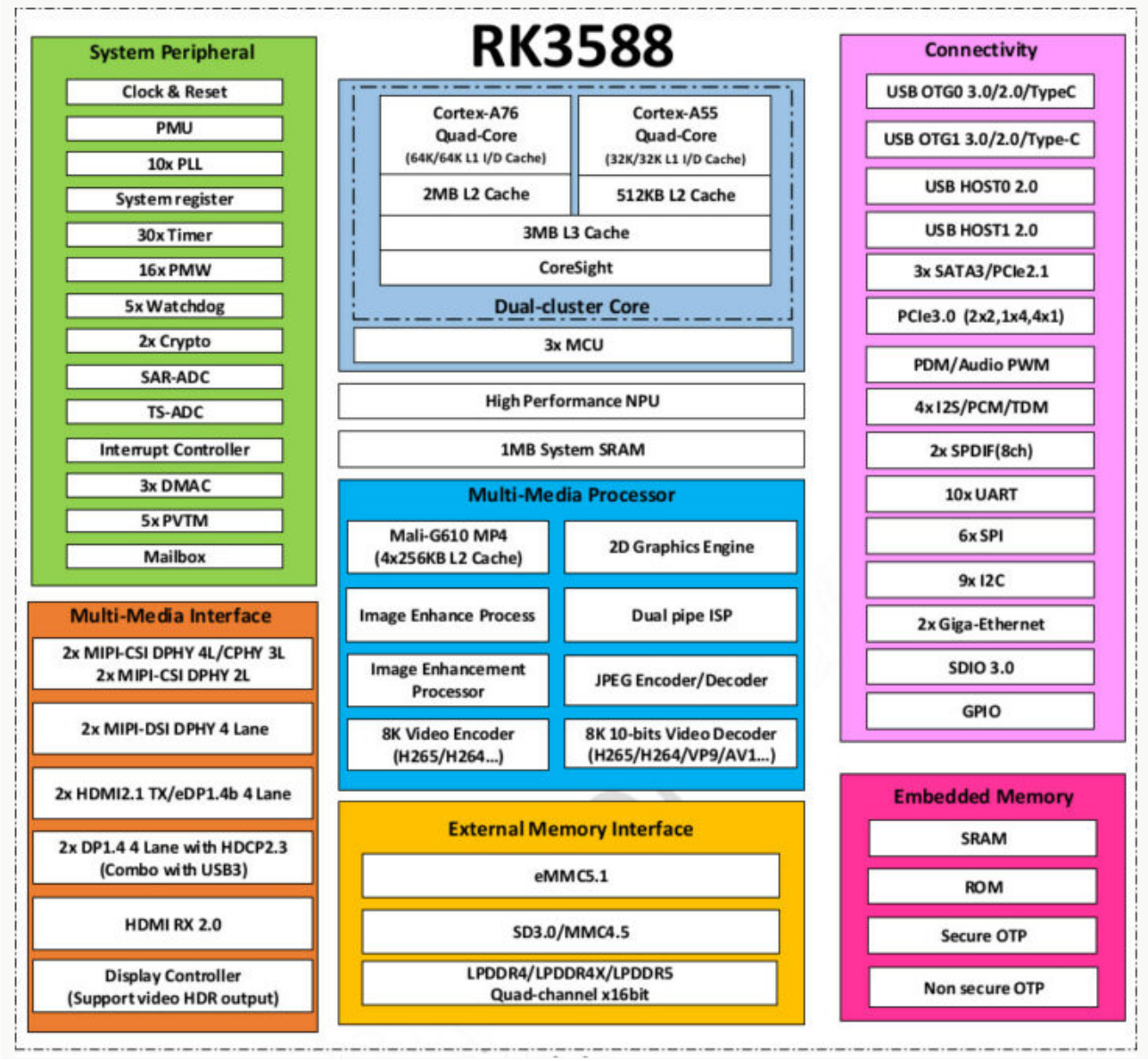


Рисунок 5: Функциональные модули Rockchip RK3588

Основные преимущества процессора:

- Встроенный графический процессор (GPU) Mali-G610 MP4 обеспечивает высокую производительность в графически интенсивных приложениях, таких как игры, виртуальная реальность и обработка изображений.
- Процессор поддерживает декодирование и кодирование видео 8K, что делает его идеальным для использования в мультимедийных приложениях, включая умные телевизоры, стриминговые устройства и медиаплееры.
- Поддержка множества интерфейсов, включая HDMI 2.1, PCIe 3.0, USB 3.2, и SATA 3.0, позволяет легко интегрировать процессор в различные системы и устройства.
- Встроенный NPU (Neural Processing Unit) обеспечивает ускорение задач машинного обучения и искусственного интеллекта, таких как распознавание лиц, голосовой интерфейс и обработка естественного языка.

- RK3588 разработан с учетом энергоэффективности, что позволяет использовать его в устройствах с ограниченным энергопотреблением, таких как портативные устройства и IoT.
- Процессор поддерживает множество операционных систем, включая Android, Linux, и другие, что обеспечивает гибкость при разработке программного обеспечения.
- Высокая производительность в многозадачных приложениях благодаря архитектуре big.LITTLE, которая позволяет эффективно распределять задачи между высокопроизводительными и энергоэффективными ядрами.
- Процессор поддерживает до 32 ГБ LPDDR4/4x памяти, обеспечивая высокую пропускную способность и быструю работу с большими объемами данных.

Расположение разъемов на плате

Вид сверху

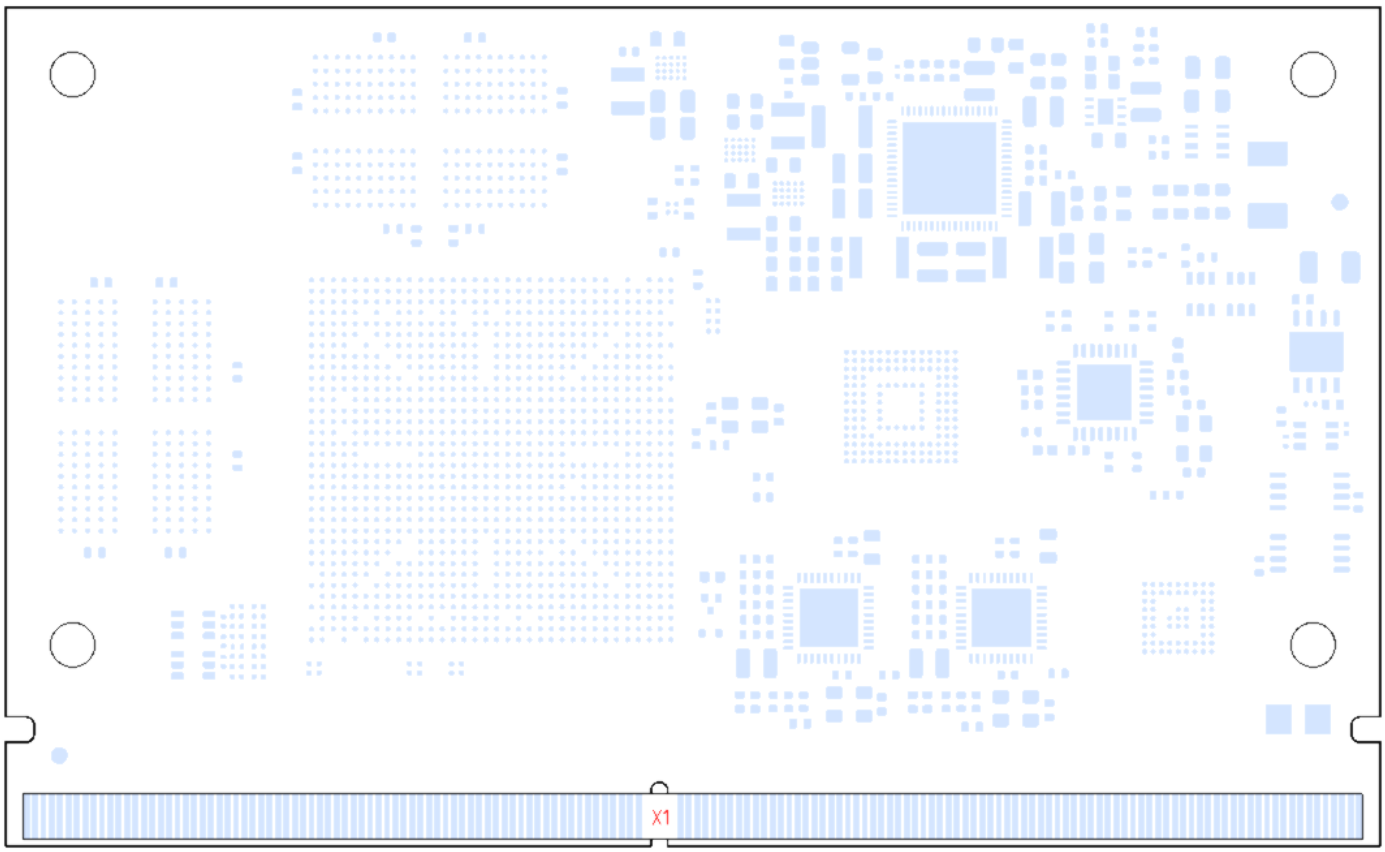


Рисунок 6: Расположение разъемов на плате. Вид сверху

Вид снизу

На нижней стороне платы разъемы отсутствуют.

Распиновка разъемов

Распиновка разъема X1 согласно SMARC

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P1	SMB_ALERT#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		SMBus Alert# (Interrupt) Signal	Standby/Sleep	
P2	GND	GND			PWR GND						
P3	CSI1_CK+	CSI_1.C0._P	AK20		CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	
P4	CSI1_CK-	CSI_1.C0._N	AL20		CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	
P5	GBE1_SDP	**NC**	-		GBE1	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P6	GBE0_SDP	**NC**	-		GBE0	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P7	CSI1_RX0+	CSI_1.D0._P	AK18		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P8	CSI1_RX0-	CSI_1.D0._N	AL18		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P9	GND	GND			PWR GND						
P10	CSI1_RX1+	CSI_1.D1._P	AK19		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P11	CSI1_RX1-	CSI_1.D1._N	AL19		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P12	GND	GND			PWR GND						
P13	CSI1_RX2+	CSI_1.D2._P	AK21		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P14	CSI1_RX2-	CSI_1.D2._N	AL21		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P15	GND	GND			PWR GND						
P16	CSI1_RX3+	CSI_1.D3._P	AK22		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P17	CSI1_RX3-	CSI_1.D3._N	AL22		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P18	GND	GND			PWR GND						
P19	GBE0_MDI3-	ETH_0.MDI3._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.10
P20	GBE0_MDI3+	ETH_0.MDI3._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.9
P21	GBE0_LINK100#	LED_0_100#	-		GBE0	O OD CMOS	3V3	PU 10K	Link Speed Indication LED for GBE0 100Mbps	Standby	D16-ETH-A.32, PU10K
P22	GBE0_LINK1000#	LED_0_1000#	-		GBE0	O OD CMOS	3V3	PU 10K	Link Speed Indication LED for GBE0 1000Mbps	Standby	D16-ETH-A.34 PU10K

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P23	GBE0_MDI2-	ETH_0.MDI2._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.7
P24	GBE0_MDI2+	ETH_0.MDI2._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.6
P25	GBE0_LINK_ACT#	LED_0_ACT#	-		GBE0	O OD CMOS	3V3	PU 10K	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	D16-ETH-A.33 PU10K
P26	GBE0_MDI1-	ETH_0.MDI1._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.5
P27	GBE0_MDI1+	ETH_0.MDI1._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.4
P28	GBE0_CTREF	Unconnected	-		GBE0	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
P29	GBE0_MDI0-	ETH_0.MDI0._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.2
P30	GBE0_MDI0+	ETH_0.MDI0._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-A.1
P31	SPI0_CS1#	SPI0_M2.CS1	E25		SPI0	O CMOS	1V8		SPI0 Master Chip Select 1	Standby	
P32	GND	GND			PWR GND						
P33	SDIO_WP	Unconnected	-		SDIO	I OD CMOS	1V8 or 3V3		SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	Runtime	
P34	SDIO_CMD	SDMMC.CMD	AE2		SDIO	I/O CMOS	1V8 or 3V3		SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	Runtime	
P35	SDIO_CD#	SDMMC_DET	P31		SDIO	I OD CMOS	1V8 or 3V3	PU 100K	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	Runtime	
P36	SDIO_CK	SDMMC.CLK	AE1		SDIO	O CMOS	1V8 or 3V3		SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	Runtime	SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
P37	SDIO_PWR_EN	SD_PWREN	P33		SDIO	O CMOS	3V3		SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	Runtime	
P38	GND	GND			PWR GND						
P39	SDIO_D0	SDMMC.D0	AD2		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P40	SDIO_D1	SDMMC.D1	AD1		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P41	SDIO_D2	SDMMC.D2	AF2		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P42	SDIO_D3	SDMMC.D3	AF1		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P43	SPI0_CS0#	SPI0_M2.CS0	E24		SPI0	O CMOS	1V8		SPI0 Master Chip Select 0	Standby	This signal can be used to select Carrier SPI as boot device
P44	SPI0_CK	SPI0_M2.CLK	D27		SPI0	O CMOS	1V8		SPI0 Clock	Standby	
P45	SPI0_DIN	SPI0_M2.MISO	D25		SPI0	I CMOS	1V8		SPI0 Master input / Slave output	Standby	also referred to as MISO
P46	SPI0_DO	SPI0_M2.MOSI	D26		SPI0	O CMOS	1V8		SPI0 Master output / Slave input	Standby	also referred to as MOSI
P47	GND	GND			PWR GND						
P48	SATA_TX+	SATA_TX_P	K33		SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P49	SATA_TX-	SATA_TX_N	K34		SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P50	GND	GND			PWR GND						
P51	SATA_RX+	SATA_RX_P	J33		SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P52	SATA_RX-	SATA_RX_N	J34		SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P53	GND	GND			PWR GND						
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	SPI4_M2.CS0	A27		SPI1	O CMOS	1V8		SPI1 Master Chip Select 0	Standby	
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	Unconnected	-		SPI1	O CMOS	1V8		SPI1 Master Chip Select 1	Standby	
P56	ESPI_CK / SPI1_CK / QSPI_CK	SPI4_M2.CLK	A26		SPI1	O CMOS	1V8		SPI1 Clock	Standby	
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	SPI4_M2.MISO	A24		SPI1	I CMOS	1V8		SPI1 Master input / Slave output	Standby	also referred to as MISO
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	SPI4_M2.MOSI	A25		SPI1	O CMOS	1V8		SPI1 Master output / Slave input	Standby	also referred to as MOSI
P59	GND	GND			PWR GND						
P60	USB0+	HOST_0.D_P	AK6		USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P61	USB0-	HOST_0.D_M	AL6		USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P62	USB0_EN_OC#	USB0_EN_OC#	-		USB0	I/O OD CMOS		PU 10K	USB Over-Current Sense for Port 0	Standby	D11.20 / D11.16 PU 10K
P63	USB0_VBUS_DET	Unconnected	-		USB0	I USB VBUS 5V	USB VBUS 5V		USB Port 0 Host Power Detection	Standby	
P64	USB0_OTG_ID	Unconnected	-		USB0				Input Pin to Announce OTG Device Insertion on USB 2.0 Port	Standby	
P65	USB1+	HOST_1.D_P	AL7		USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P66	USB1-	HOST_1.D_M	AM7		USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P67	USB1_EN_OC#	USB1_EN_OC#	-		USB1	I/O OD CMOS		PU 10K	USB Over-Current Sense for Port 1	Standby	D11.19 / D11.15 PU 10K
P68	GND	GND			PWR GND						
P69	USB2+	OTG_1_D_P	AK9		USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P70	USB2-	OTG_1_D_N	AL9		USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P71	USB2_EN_OC#	USB2_EN_OC#	-		USB2	I/O OD CMOS		PU 10K	USB Over-Current Sense for Port 2	Standby	D11.18 / D11.14 PU 10K
P72	RSVD	Unconnected	-								
P73	RSVD	Unconnected	-								
P74	USB3_EN_OC#	USB3_EN_OC#	-		USB3	I/O OD CMOS		PU 10K	USB Over-Current Sense for Port 3	Standby	D11.17 / D11.13 PU 10K
P75	PCIE_A_RST#	PCIE_A_PERST	AJ27		PCIEA	O CMOS			PCIe Port A reset output	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P76	USB4_EN_OC#	Unconnected	-		USB4	I/O OD CMOS			USB Over-Current Sense for Port 4	Standby	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P77	PCIE_B_CKREQ#	PCIE_B_CKREQ	-		PCIEB	IO OD CMOS			PCIe Port B clock request	Runtime	D1.17
P78	PCIE_A_CKREQ#	PCIE_A_CKREQ	-		PCIEA	IO OD CMOS			PCIe Port A clock request	Runtime	D1.12
P79	GND	GND			PWR GND						
P80	PCIE_C_REFCK+	NC	-		PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P81	PCIE_C_REFCK-	NC	-		PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P82	GND	GND			PWR GND						
P83	PCIE_A_REFCK+	PCIE3_A_REFCLK._P	-		PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	D1.14
P84	PCIE_A_REFCK-	PCIE3_A_REFCLK._N	-		PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	D1.13
P85	GND	GND			PWR GND						
P86	PCIE_A_RX+	PCIE_A_RX_P	G33		PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P87	PCIE_A_RX-	PCIE_A_RX_N	G34		PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P88	GND	GND			PWR GND						
P89	PCIE_A_TX+	PCIE_A_TX_P	D32		PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P90	PCIE_A_TX-	PCIE_A_TX_N	D33		PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P91	GND	GND			PWR GND						
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX_0.D2._P	AL24 / AL2		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX_0.D2._N	AL24 / AL1		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P94	GND	GND			PWR GND						
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX_0.D1._P	AL24 / AK3		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX_0.D1._N	AL24 / AK2		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P97	GND	GND			PWR GND						
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX_0.D0._P	AJ2		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX_0.D0._N	AJ1		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P100	GND	GND			PWR GND						
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX_0.D3._P	AH3		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX_0.D3._N	AH2		HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P103	GND	GND			PWR GND						
P104	HDMI_HPD / DP1_HPD	HDMI_TX0_HPD	B26		HDMI	I CMOS	1V8		HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	Runtime	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI0_I2C.SCL	AJ24		HDMI	I/O OD CMOS	1V8	PU 2K2	I2C_CLK Line Dedicated to HDMI	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI0_I2C.SDA	AH24		HDMI	I/O OD CMOS	1V8	PU 2K2	I2C_DAT Line Dedicated to HDMI	Runtime	
P107	DP1_AUX_SEL	Unconnected	-		DP1++_HDMI	I CMOS	1V8		Strapping Signal to Enable Either HDMI or DP Output	Runtime	0 - DP 1 - HDMI
P108	GPIO0 / CAM0_PWR#	GPIO0	E30		GPIO	I/O CMOS	1V8		GPIO Pin 0 Preferred Output	Runtime	Shared with CAM0_PWR#
P109	GPIO1 / CAM1_PWR#	GPIO1	D29		GPIO	I/O CMOS	1V8		GPIO Pin 1 Preferred Output	Runtime	Shared with CAM1_PWR#
P110	GPIO2 / CAM0_RST#	GPIO2	AB30		GPIO	I/O CMOS	1V8		GPIO Pin 2 Preferred Output	Runtime	Shared with CAM0_RST#
P111	GPIO3 / CAM1_RST#	GPIO3	AB31		GPIO	I/O CMOS	1V8		GPIO Pin 3 Preferred Output	Runtime	Shared with CAM1_RST#
P112	GPIO4 / HDA_RST#	GPIO4	AD30		GPIO	I/O CMOS	1V8		GPIO Pin 4 Preferred Output	Runtime	
P113	GPIO5 / PWM_OUT	PWM1_M1	E28		GPIO	I/O CMOS	1V8		GPIO Pin 5 Preferred Output	Runtime	
P114	GPIO6 / TACHIN	GPIO6	AC30		GPIO	I/O CMOS	1V8		GPIO Pin 6 Preferred Output	Runtime	
P115	GPIO7	GPIO7	AE30		GPIO	I/O CMOS	1V8		GPIO Pin 7 Preferred Output	Runtime	
P116	GPIO8	GPIO8	Y27		GPIO	I/O CMOS	1V8		GPIO Pin 8 Preferred Output	Runtime	
P117	GPIO9	GPIO9	AE29		GPIO	I/O CMOS	1V8		GPIO Pin 9 Preferred Output	Runtime	
P118	GPIO10	GPIO10	AG23		GPIO	I/O CMOS	1V8		GPIO Pin 10 Preferred Output	Runtime	
P119	GPIO11	GPIO11	C24		GPIO	I/O CMOS	1V8		GPIO Pin 11 Preferred Output	Runtime	
P120	GND	GND			PWR GND						
P121	I2C_PM_CK	I2C_PM.SCL	W31		MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus CLK	Standby/Sleep	
P122	I2C_PM_DAT	I2C_PM.SDA	V31		MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus DATA	Standby/Sleep	
P123	BOOT_SEL0#	BOOTSEL_0	AM16		BOOT	I OD CMOS	1V8	PU 100K	Input straps determine the Module boot device.	Standby	
P124	BOOT_SEL1#	NC	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P125	BOOT_SEL2#	NC	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P126	RESET_OUT#	RESET_OUT	U33		MANAGEMENT	O CMOS	1V8		General purpose reset output to Carrier Board.	Standby	
P127	RESET_IN#	RESET_L	M31		MANAGEMENT	I OD CMOS	1V8...5V	PU 10K	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal Shall be level triggered during bootup to allow to stop booting of the module. After bootup it May act as an edge triggered signal.	Standby	
P128	POWER_BTN#	PWRON_KEY	-		MANAGEMENT	I OD CMOS	1V8...5V	PU 10K	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Sleep	U2.4 (100R)
P129	SER0_TX	UART1_M1.TXD	E26		SER0	O CMOS	1V8		Asynchronous Serial Data Output Port 0	Runtime	
P130	SER0_RX	UART1_M1.RXD	E27		SER0	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 0	Runtime	
P131	SER0_RTS#	UART1_M1.RTS	F24		SER0	O CMOS	1V8		Request to Send Handshake Line for Port 0	Runtime	
P132	SER0_CTS#	UART1_M1.CTS	F25		SER0	I CMOS	1V8	PU 100K	Clear to Send Handshake Line for Port 0	Runtime	
P133	GND	GND			PWR GND						

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
P134	SER1_TX	UART2_M0.TXD	P29		SER1	O CMOS	1V8		Asynchronous Serial Data Output Port 1	Runtime	
P135	SER1_RX	UART2_M0.RXD	R29		SER1	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 1	Runtime	
P136	SER2_TX	UART9_M2.TXD	AB28		SER2	O CMOS	1V8		Asynchronous Serial Data Output Port 2	Runtime	
P137	SER2_RX	UART9_M2.RXD	AA27		SER2	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 2	Runtime	
P138	SER2_RTS#	UART9_M2.RTS	AG25		SER2	O CMOS	1V8		Request to Send Handshake Line for Port 2	Runtime	
P139	SER2_CTS#	UART9_M2.CTS	AG24		SER2	I CMOS	1V8		Clear to Send Handshake Line for Port 2	Runtime	
P140	SER3_TX	SER3.TXD	G27		SER3	O CMOS	1V8		Asynchronous Serial Data Output Port 3	Runtime	
P141	SER3_RX	SER3.RXD	G29		SER3	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 3	Runtime	
P142	GND	GND			PWR GND						
P143	CAN0_TX	CAN0.TXD	AH25		CAN0	O CMOS	1V8		CAN Port 0 Transmit Output	Runtime	
P144	CAN0_RX	CAN0.RXD	AH26		CAN0	I CMOS	1V8		CAN Port 0 Receive Input	Runtime	
P145	CAN1_TX	CAN1.TXD	-		CAN1	O CMOS	1V8		CAN Port 1 Transmit Output	Runtime	D8.7
P146	CAN1_RX	CAN1.RXD	-		CAN1	I CMOS	1V8		CAN Port1 Receive Input	Runtime	D9.7
P147	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P148	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P149	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P150	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P151	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P152	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P153	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P154	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P155	VDD_IN	VCC_5V0			PWR		3V...5.25V				
P156	VDD_IN	VCC_5V0			PWR		3V...5.25V				
S1	CSI1_TX+ / I2C_CAM1_CK	I2C_CAM1.SCL	AA28		CSI1	I/O OD CMOS	1V8	PU 2K2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0
S2	CSI1_TX- / I2C_CAM1_DAT	I2C_CAM1.SDA	Y29		CSI1	I/O OD CMOS	1V8	PU 2K2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S3	GND	GND			PWR GND						
S4	RSVD	Unconnected	-								
S5	CSI0_TX+ / I2C_CAM0_CK	I2C_CAM0.SCL	F26		CSI0	I/O OD CMOS	1V8	PU 2K2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0
S6	CAM_MCK	MIPI_CAMERA1_CLK_M1	AH27		CSI	O CMOS	1V8		Master clock output	Runtime	
S7	CSI0_TX- / I2C_CAM0_DAT	I2C_CAM0.SDA	F27		CSI0	I/O OD CMOS	1V8	PU 2K2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S8	CSI0_CK+	CSI_0.C0._P	AN32		CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S9	CSI0_CK-	CSI_0.C0._N	AP31		CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S10	GND	GND			PWR GND						
S11	CSI0_RX0+	CSI_0.D0._P	AN29		CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S12	CSI0_RX0-	CSI_0.D0._N	AP29		CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S13	GND	GND			PWR GND						
S14	CSI0_RX1+	CSI_0.D1._P	AN30		CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S15	CSI0_RX1-	CSI_0.D1._N	AP30		CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S16	GND	GND			PWR GND						
S17	GBE1_MDI0+	ETH_1.MDI0._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.1
S18	GBE1_MDI0-	ETH_1.MDI0._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.2
S19	GBE1_LINK100#	LED_1_100#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 100Mbps	Standby	D16-ETH-B.32 PU 10K
S20	GBE1_MDI1+	ETH_1.MDI1._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.4
S21	GBE1_MDI1-	ETH_1.MDI1._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.5
S22	GBE1_LINK1000#	LED_1_1000#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 1000Mbps	Standby	D16-ETH-B.34 PU 10K
S23	GBE1_MDI2+	ETH_1.MDI2._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.6
S24	GBE1_MDI2-	ETH_1.MDI2._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.7
S25	GND	GND			PWR GND						
S26	GBE1_MDI3+	ETH_1.MDI3._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.9
S27	GBE1_MDI3-	ETH_1.MDI3._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	D16-ETH-B.10
S28	GBE1_CTREF	Unconnected	-		GBE1	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
S29	PCIE_D_TX+ / SERDES_0_TX+	PCIE_D_TX_P	C29		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S30	PCIE_D_TX- / SERDES_0_TX-	PCIE_D_TX_N	B29		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S31	GBE1_LINK_ACT#	LED_1_ACT#	-		GBE1	O OD CMOS	3V3		Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	D16-ETH-B.33 PU 10K
S32	PCIE_D_RX+ / SERDES_0_RX+	PCIE_D_RX_P	C31		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S33	PCIE_D_RX- / SERDES_0_RX-	PCIE_D_RX_N	B31		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S34	GND	GND			PWR GND						
S35	USB4+	NC	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S36	USB4-	NC	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S37	USB3_VBUS_DET	OTG_0_VBUS	AM14		USB3	I USB VBUS 5V	USB VBUS 5V		USB Port 3 Host Power Detection	Standby	
S38	AUDIO_MCK	I2S0.MCK	F30		I2S	O CMOS	1V8		Master Clock Output to I2S Codec(s)	Runtime	
S39	I2S0_LRCK	I2S0.LRCK	D30		I2S0	I/O CMOS	1V8		I2S0 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S40	I2S0_SDOUT	I2S0.SDOUT	E29		I2S0	O CMOS	1V8		I2S0 Digital Audio Output	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S41	I2S0_SDIN	I2S0.SDIN	D28		I2S0	I CMOS	1V8		I2S0 Digital Audio Input	Runtime	
S42	I2S0_CK	I2S0.CLK	E31		I2S0	I/O CMOS	1V8		I2S0 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S43	ESPI_ALERT0#	ESPI_ALERT0	C25		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	
S44	ESPI_ALERT1#	ESPI_ALERT1	C27		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	
S45	MDIO_CLK	Unconnected	-		SERDES	O CMOS	1V8		MDIO Signals to Configure Possible PHYs		
S46	MDIO_DAT	Unconnected	-		SERDES	I/O OD CMOS	1V8		MDIO Signals to Configure Possible PHYs		
S47	GND	GND			PWR GND						
S48	I2C_GP_CK	I2C_GP.SCL	T31		I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Clock Signal	Runtime	
S49	I2C_GP_DAT	I2C_GP.SDA	T28		I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Data Signal	Runtime	
S50	HDA_SYNC / I2S2_LRCK	Unconnected	-		I2S2	I/O CMOS	1V8		I2S2 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S51	HDA_SDO / I2S2_SDOUT	Unconnected	-		I2S0	O CMOS	1V8		I2S2 Digital Audio Output	Runtime	
S52	HDA_SDI / I2S2_SDIN	Unconnected	-		I2S0	I CMOS	1V8		I2S2 Digital Audio Input	Runtime	
S53	HDA_CK / I2S2_CK	Unconnected	-		I2S0	I/O CMOS	1V8		I2S2 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S54	SATA_ACT#	SATA1_ACT	AJ28		SATA	O OD CMOS	3V3		SATA Activity Indicator	Runtime	Shall be able to sink 24mA or more Carrier LED current
S55	USB5_EN_OC#	Unconnected	-		USB5	I/O OD CMOS	3V3		USB Over-Current Sense for Port 5	Standby	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
S56	ESPI_IO_2 / QSPI_IO_2	Unconnected	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S57	ESPI_IO_3 / QSPI_IO_3	Unconnected	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S58	ESPI_RESET#	Unconnected	-		eSPI	O CMOS	1V8		ESPI Reset	Standby	
S59	USB5+	NC	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S60	USB5-	NC	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S61	GND	GND			PWR GND						
S62	USB3_SSTX+	USB3_OTG0_SS.D_TX._P	AP14		USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S63	USB3_SSTX-	USB3_OTG0_SS.D_TX._N	AN14		USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S64	GND	GND			PWR GND						
S65	USB3_SSRX+	USB3_OTG0_SS.D_RX._P	AN13		USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S66	USB3_SSRX-	USB3_OTG0_SS.D_RX._N	AP13		USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S67	GND	GND			PWR GND						
S68	USB3+	OTG_0_D_P	AL12		USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S69	USB3-	OTG_0_D_N	AM12		USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S70	GND	GND			PWR GND						
S71	USB2_SSTX+	USB3_OTG1_SS.D_TX._P	AP9		USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S72	USB2_SSTX-	USB3_OTG1_SS.D_TX._N	AN9		USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S73	GND	GND			PWR GND						
S74	USB2_SSRX+	USB3_OTG1_SS.D_RX._P	AN8		USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S75	USB2_SSRX-	USB3_OTG1_SS.D_RX._N	AP8		USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S76	PCIE_B_RST#	PCIE_B_PERST	AK27		PCIEB	O CMOS	3V3		PCIe Port B reset output	Runtime	
S77	PCIE_C_RST#	PCIE_C_PERST	AM29		PCIEC	O CMOS	3V3		PCIe Port C reset output	Runtime	
S78	PCIE_C_RX+ / SERDES_1_RX+	PCIE_C_RX_P	B32		PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S79	PCIE_C_RX- / SERDES_1_RX-	PCIE_C_RX_N	A32		PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S80	GND	GND			PWR GND						
S81	PCIE_C_TX+ / SERDES_1_TX+	PCIE_C_TX_P	B30		PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S82	PCIE_C_TX- / SERDES_1_TX-	PCIE_C_TX_N	A30		PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S83	GND	GND			PWR GND						
S84	PCIE_B_REFCK+	PCIE3_B_REFCLK._P	-		PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	D1.18
S85	PCIE_B_REFCK-	PCIE3_B_REFCLK._N	-		PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	D1.19
S86	GND	GND			PWR GND						
S87	PCIE_B_RX+	PCIE_B_RX_P	F32		PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S88	PCIE_B_RX-	PCIE_B_RX_N	F33		PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S89	GND	GND			PWR GND						
S90	PCIE_B_TX+	PCIE_B_TX_P	C33		PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S91	PCIE_B_TX-	PCIE_B_TX_N	C34		PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S92	GND	GND			PWR GND						
S93	DP0_LANE0+	DPORT1.D0._P	AN4		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S94	DP0_LANE0-	DPORT1.D0._N	AP4		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S95	DP0_AUX_SEL	Unconnected	-		DP0++	I CMOS			Auxiliary Selection	Runtime	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S96	DP0_LANE1+	DPORT1.D1._P	AM5		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S97	DP0_LANE1-	DPORT1.D1._N	AN5		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S98	DP0_HPD	DP0_HPD	P30		DP0++	I CMOS			DP Hot Plug Detect Input	Runtime	
S99	DP0_LANE2+	DPORT1.D2._P	AN6		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S100	DP0_LANE2-	DPORT1.D2._N	AP6		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S101	GND	GND			PWR GND						
S102	DP0_LANE3+	DPORT1.D3._P	AM3		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S103	DP0_LANE3-	DPORT1.D3._N	AN3		DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S104	USB3_OTG_ID	OTG_0_ID	AL14		USB3	I CMOS			Input Pin to Announce OTG Device Insertion on USB 3.2 Port	Standby	
S105	DP0_AUX+	DPORT1.CLK._P	AN2		DP0++	I/O DP			Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S106	DP0_AUX-	DPORT1.CLK._N	AP2		DP0++	I/O DP			Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S107	LCD1_BKLT_EN	LCD1_BKLT_EN	-		eDP1	O CMOS			Secondary LVDS Channel Backlight Enable	Runtime	D11.5
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS_B.CLK._P	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	U7.B6
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS_B.CLK._N	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	U7.A6
S110	GND	GND			PWR GND						
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS_B.D0._P	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.B3
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS_B.D0._N	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.A3
S113	eDP1_HPD / DSI1_TE	Unconnected	-		DSI1	I CMOS	1V8		Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	Runtime	
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS_B.D1._P	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.B4
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS_B.D1._N	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.A4
S116	LCD1_VDD_EN	LCD1_VDD_EN	-		DSI1	O CMOS	1V8		Secondary Panel Power Enable	Runtime	D11.7
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS_B.D2._P	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.B5
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS_B.D2._N	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.A5
S119	GND	GND			PWR GND						
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS_B.D3._P	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.B7
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS_B.D3._N	-		DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	U7.A7

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S122	LCD1_BKLT_PWM	PWM0_M1	F28		DSI1	O CMOS	1V8		Secondary Panel Brightness Control	Runtime	
S123	GPIO13	GPIO13	G26		GPIO	I/O CMOS	1V8		GPIO Pin 13 Preferred Output	Runtime	
S124	GND	GND			PWR GND						
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS_A.D0._P	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.C8
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS_A.D0._N	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.C9
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	-		DSI0	O CMOS	1V8		Primary Panel Backlight Enable	Runtime	D11.4
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS_A.D1._P	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.D8
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS_A.D1._N	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.D9
S130	GND	GND			PWR GND						
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS_A.D2._P	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.E8
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS_A.D2._N	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.E9
S133	LCD0_VDD_EN	LCD0_VDD_EN	-		DSI0	O CMOS	1V8		Primary Panel Power Enable	Runtime	D11.6
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS_A.CLK._P	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	U7.F8
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS_A.CLK._N	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	U7F9
S136	GND	GND			PWR GND						
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS_A.D3._P	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.G8
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS_A.D3._N	-		DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	U7.G9
S139	I2C_LCD_CK	I2C_LCD.SCL	AJ25		DSI	I\O OD CMOS			I2C clock to read LCD display EDID EEPROMs	Runtime	
S140	I2C_LCD_DAT	I2C_LCD.SDA	AK24		DSI	I\O OD CMOS			DDC Data Line Used for Flat Panel Detection and Control	Runtime	
S141	LCD0_BKLT_PWM	PWM4_M1	AF34		DSI0	O CMOS			Primary Panel Brightness Control	Runtime	
S142	GPIO12	GPIO12	B25		GPIO	I/O CMOS			GPIO Pin 12 Preferred Output	Runtime	
S143	GND	GND			PWR GND						
S144	eDP0_HPD / DSI0_TE	Unconnected	-		DSI0	I CMOS	1V8		Primary DSI Panel Tearing Effect Signal	Runtime	
S145	WDT_TIME_OUT#	WDT_TIME_OUT#	K29		WATCHDOG	O CMOS	1V8		Watch-Dog-Timer Output, low active	Runtime	
S146	PCIE_WAKE#	PCIE_WAKE_N	AK27, AL28, AL30, AM27		PCIE	I OD CMOS	3V3		PCIe wake up interrupt to host – common to PCIe links A, B, C, D	Standby	
S147	VDD_RTC	VBAT	-		PWR RTC		2V...3.25V				D7.3
S148	LID#	Unconnected	-		MANAGEMENT	I OD CMOS	1V8...5V		Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	Standby	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S149	SLEEP#	Unconnected	-		MANAGEMENT	I OD CMOS	1V8...5V		Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Standby	
S150	VIN_PWR_BAD#	VIN_GOOD	-		MANAGEMENT	I OD CMOS	VDD_IN		Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.		U6.1
S151	CHARGING#	Unconnected	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	Standby/Sleep	
S152	CHARGER_PRSNT#	Unconnected	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier if DC input for battery charger is present	Standby/Sleep	
S153	CARRIER_STBY#	CARRIER_STBY#	-		MANAGEMENT	O CMOS	1V8		The Module shall drive this signal low when the system is in a standby power state.	Standby	U2.39, D5.7 (100R)
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	-		MANAGEMENT	O CMOS	1V8		Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	Standby	U2.39, D5.7 (100R)
S155	FORCE_RECOV#	FORCE_RECOV	AM16		BOOT	I OD CMOS	1V8	PU 100K	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	Standby	
S156	BATLOW#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Battery low indication to Module. Carrier to float the line in inactive state.	Standby/Sleep	

Pin #	Name STANDART	Signals_SM_RK3588	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3588	Description	Power Domain	Comments
S157	TEST#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Held Low by Carrier to Invoke Module Vendor Specific Test Functions	Standby/Sleep	
S158	GND	GND			PWR GND						

Информация для заказа