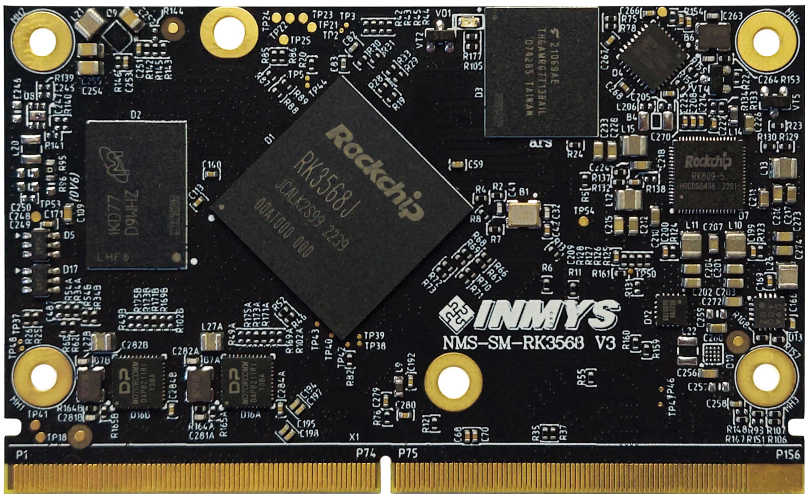
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NMS-SM-RK3568 v4 ds-ru



Процессорный модуль **NMS-SM-RK3568** выполнен на основе четырехъядерного 64-битного процессора Cortex-A55 RK3568 производства **Rockchip**, который оснащен двухъядерным графическим процессором и высокопроизводительным NPU, поддерживающим до 8 ГБ ОЗУ.

Модуль выполнен в формате стандарта SMARC,обладает хорошей вычислительной мощностью и богатым набором интерфейсов, что позволяет использовать его для энергоэффективных и высокопроизводительных вычислительных систем: он может использоваться на транспорте, в системах защиты информации, в мультимедийных системах, в системах промышленной автоматизации, в автомобильной промышленности, в медицинской технике, в системах передачи данных, банковских терминалах, в приборостроении, также может использоваться в системах интернета вещей на уровне шлюзов и Edge-контроллеров, как часть систем управления и современных расширяемых технологий, как часть мультимедиа устройств для управления аудио- и видеоконтентом и т.д.

NMS-SM-RK3568 использует передовую 22-нм технологию, основная частота до 2,0 ГГц, что обеспечивает эффективную и стабильную производительность обработки данных, ЦП может быть оснащен памятью объемом до 8 ГБ, шириной до 32 бит и частотой до 1600 МГц, поддерживается режим ECC, что делает данные более безопасными и надежными, а также отвечает требованиям сценариев приложений с большой памятью, в то же время он объединяет двухъядерную архитектуру GPU и высокопроизводительные VPU и NPU. GPU поддерживает OpenGL ES3.2 / 2.0 / 1.1, Vulkan1.1, VPU может обеспечивать декодирование видео 4K 60fps H.265 / H.264 / VP9 и кодирование видео 1080P 100fps H.265 / H.264, NPU поддерживает Caffe / TensorFlow и т.д.

RK3568 имеет MIPI-CSI, MIPI-DSI, HDMI2.0, видеоинтерфейс EDP, может поддерживать до трех экранов с различным выводом на дисплей, а встроенный процессор сигналов изображения ISP 8M может поддерживать двойную камеру и функцию HDR.

Модуль поддерживает конфигурацию двойных гигабитных адаптивных портов Ethernet RJ45, которые могут получать доступ и передавать внутренние и внешние сетевые данные через двойные сетевые порты для повышения эффективности сетевой

передачи.

Платформа **NMS-SM-RK3568** поддерживает Android, операционную систему Ubuntu, система стабильна и надежна, а также обеспечивает безопасную и стабильную системную среду для исследования и производства продукции.

Плата оснащена интерфейсом SMARC, по стандарту (2.0\2.1), который в сочетании с основной платой может формировать полноценную высокопроизводительную материнскую плату для промышленного применения. Он имеет более богатые интерфейсы расширения и может быть напрямую применен к различным интеллектуальным продуктам, ускоряя продвижение продукта.

Модуль создан на доступной несанкционной компонентной базе и позволяет стабильно и регулярно выпускать промышленные партии изделий.

Краткое описание возможностей

Таблица 1: Основные технические характеристики

Внешние разъемы	Краевой разъём в соответствии со SMARC, по стандарту (2.0\2.1)
Процессор	RK3568
	Ядра:4х-ядерный 64х-битный Cortex-A55, 22нм техпроцесс, частота до 2.0ГГц
	Графический ускоритель: ARM G52 2EE, поддержка OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, Vulkan 1.1
	Видеоускоритель: аппаратное декодирование 4K 60к/с H.265/H.264/VP9, аппаратное кодирование 1080P 100к/с H.265/H.264, 8M ISP, HDR
	Нейросопроцессор: 0.8Tops@INT8, интегрированнный высокопроизводительный AI ускоритель RKNN NPU, поддержка Caffe/TensorFlow/TFLite/ONNX/PyTorch/Keras/Darknet
ОЗУ	Память LPDDR4 2 ГБайт (512Mbit x 32) (MT53D512M32D2DS-053WT:D)
Флэш-память	Память eMMC 16 ГБайт (THGAMRG7T13BAIL)
ЭСППЗУ	2 Кбита, доступ по I2C, уникальный идентификатор 48 бит (24AA025)
ИС управления питанием	PMIC (RK809-5)
Прочие компоненты	Часы реального времени RTC (PCF8523TK)
	2х Гигабит ETH PHY (DAP8211RI)
	PCIe Gen 4 Clock Generator (PI6CG184Q2)
	Переключатель SATA → USB3 1:2 (CBTL02043A)
	Аналоговый 4-канальный переключатель SPDT 2:1 (RS2299XTQC16)
Интерфейсы	2x USB 2.0
	1x USB 3.0 OTG
	1x USB 2.0 либо 1x USB 3.0 (USB3_ HOST1_SS замультиплексирован с SATA1)
	1x PCIe 2.1
	2x PCIe 3.0
	2x CAN
	3x UART + 1x отладочный UART
	2x SPI
	3x I2C
	1x I2S
	2x PWM
	1x SATA (замультиплексирован с USB3_ HOST1_SS)
	1x HDMI
	1x eDP
	1x MIPI DSI or LVDS
	1x SDIO
	2x ETH 1GB
	20x GPIO
Напряжение питания	+5 Вольт

Потребление	**TBD**
Габаритные размеры	82×50 мм

Файлы для загрузки

Таблица 2: Файлы для загрузки

Название документа	Краткое описание	Версия	Дата
nms-sm-evm_v1_prod_sch.pdf	Схема электрическая принципиальная NMS-SM-EVM v1	v1	2022.09.15
nms-sm-rk3568_v4_plastic_1mm.zip	STEP-файл модуля NMS-SM-RK3568 v4	v4	2026.10.02

Структурная схема модуля

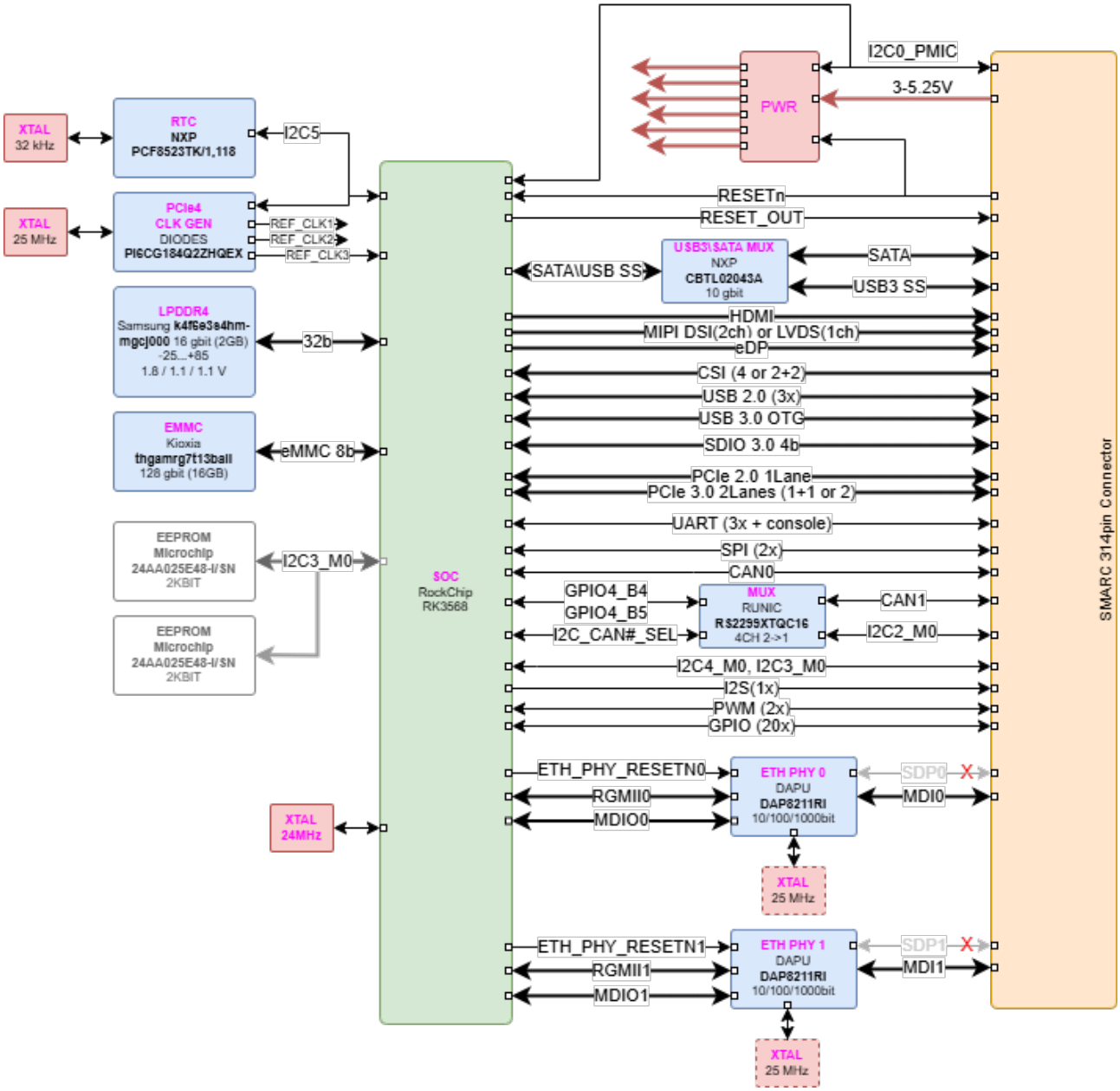


Рисунок 1: Структурная схема модуля

Механические характеристики

Размер платы : 82 x 50 мм.

Печатная плата состоит из 8 слоев, часть из которых являются заземляющими для подавления помех.

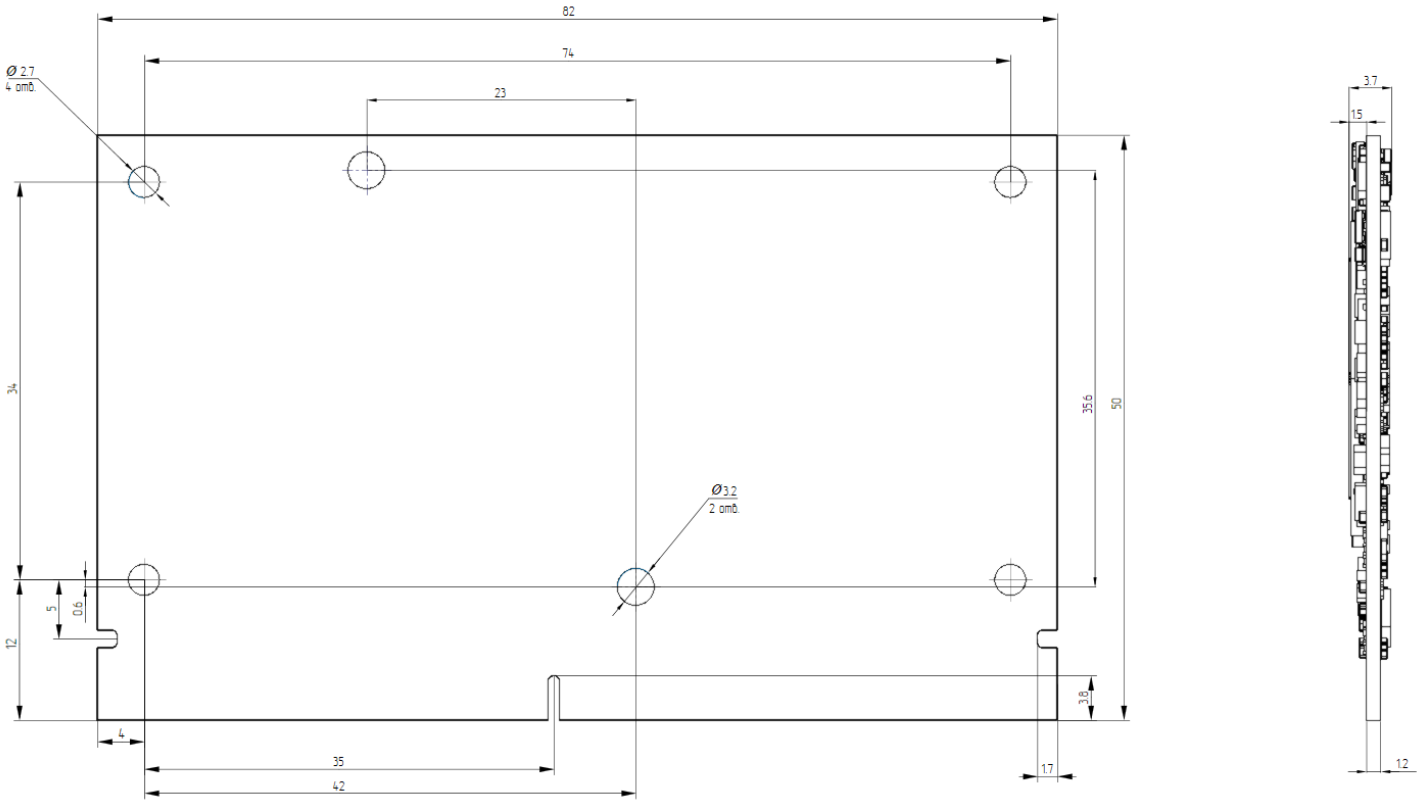


Рисунок 2: Габаритные размеры

Основные аппаратные компоненты

Расположение компонентов на плате

Вид сверху

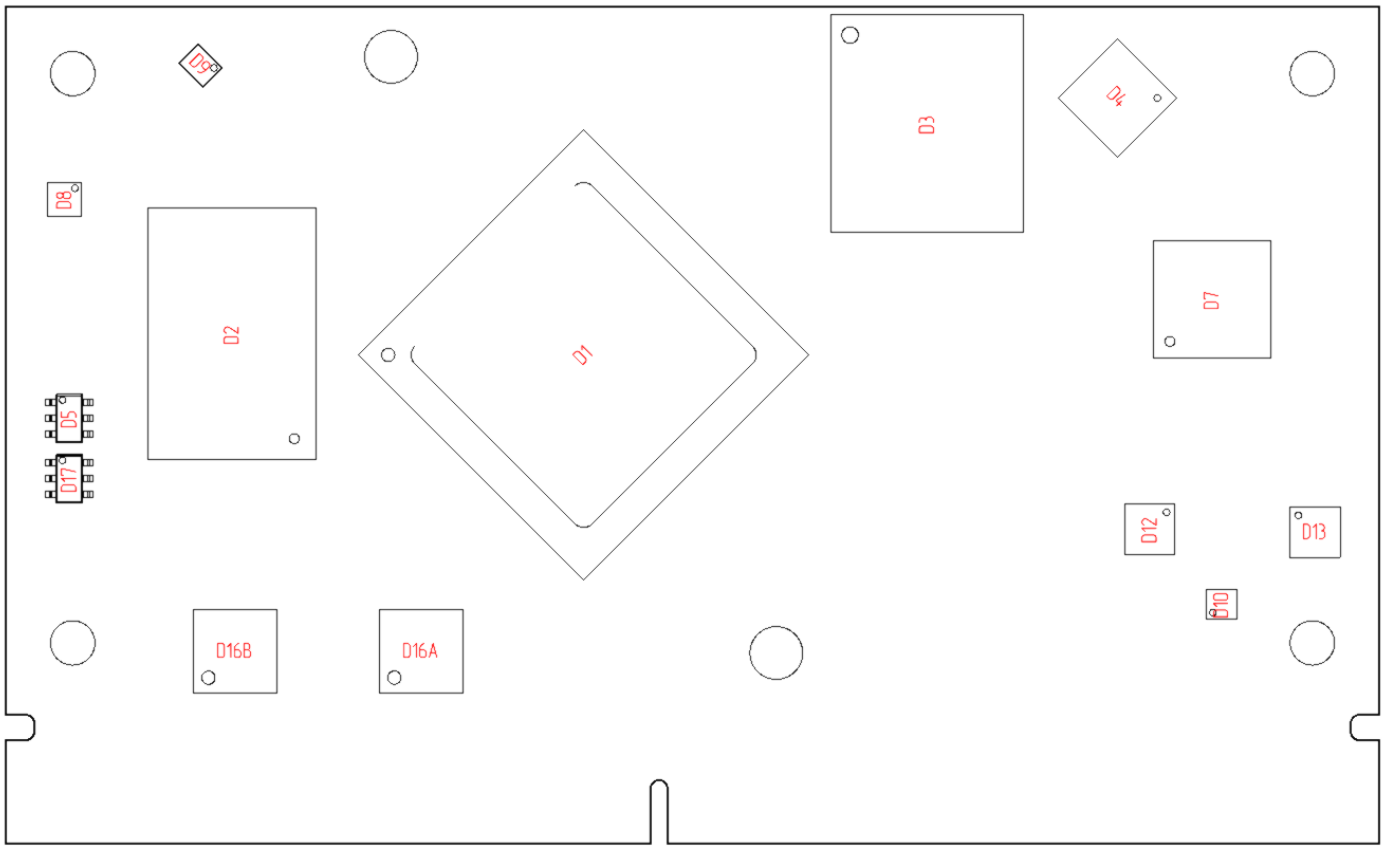


Рисунок 3: Расположение компонентов на плате. Вид сверху

Таблица 3: Наименование компонентов на плате на верхней стороне

Позиционное обозначение	P/N	Описание
D1	RK3568	CPU
D2	MT53D512M32D2DS-053WT:D	LPDDR4
D3	THGAMRG7T13BAIL	EMMC
D4	PI6CG184Q2ZHQEX	PCIe CLK GEN
D5	24AA025E48-I/SN	EEPROM 2KBIT
D7	RK809-5	PMIC
D8	PAM2305CGFADJ	DCDC BUCK
D9	FAN53200UC35X	DCDC BUCK
D10	FAN48623UC50X	DCDC BOOST
D12	RS2299XTQC16	MUX 4CH 2:1
D13	BD9A400MUV_	DCDC BUCK
D16A, D16B	DAP8211RI	ETH PHY 10/100/1000
D17	24AA025E48-I/SN	EEPROM 2KBIT

Вид снизу

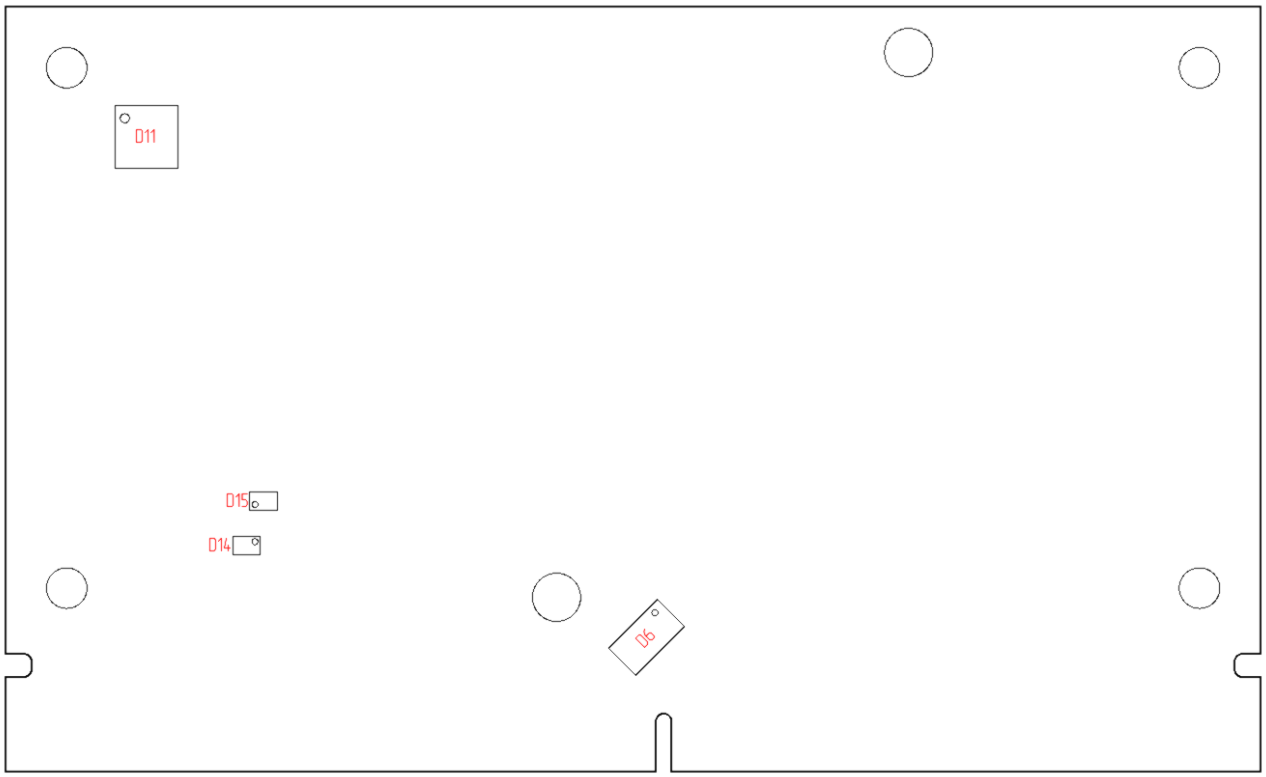


Рисунок 4: Расположение компонентов на плате. Вид снизу

Таблица 4: Наименование компонентов на плате на нижней стороне

Позиционное обозначение	P/N	Описание
D6	CBTL02043ABQ.115	SATA →USB3 1:2 SW
D11	PCF8523TK/1.118	RTC
D14, D15	NLSV2T244MUTAG	LOGIC BUF

Процессор

На рисунке 5 показаны функциональные модули в процессорной системе RK3568.

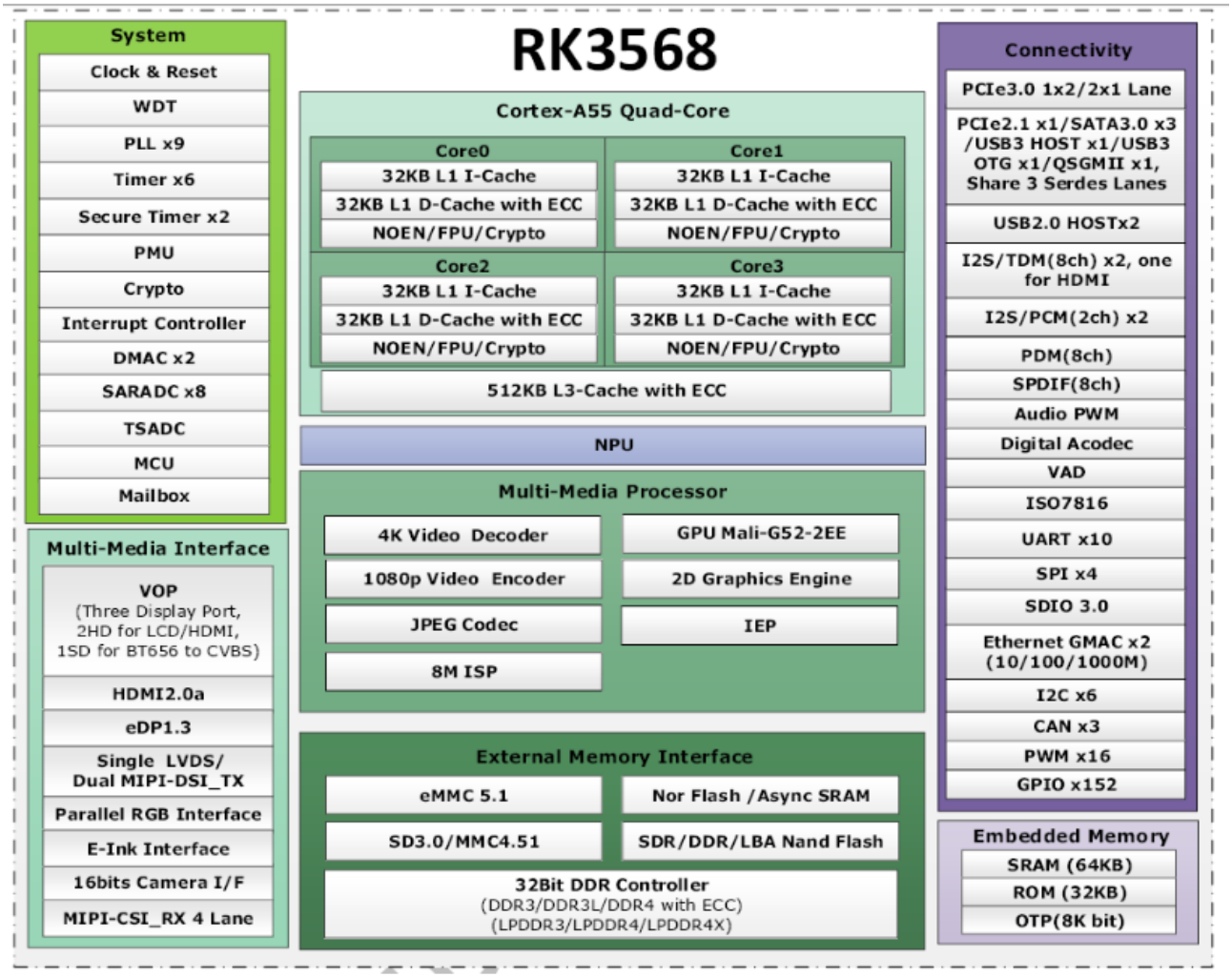


Рисунок 5: Функциональные модули Rockchip RK3568

Интерфейсы

I2C

На плате **NMS-SM-RK3568** доступно три внешних интерфейса I2C и два внутренних для взаимосвязи процессора и периферийных устройств.

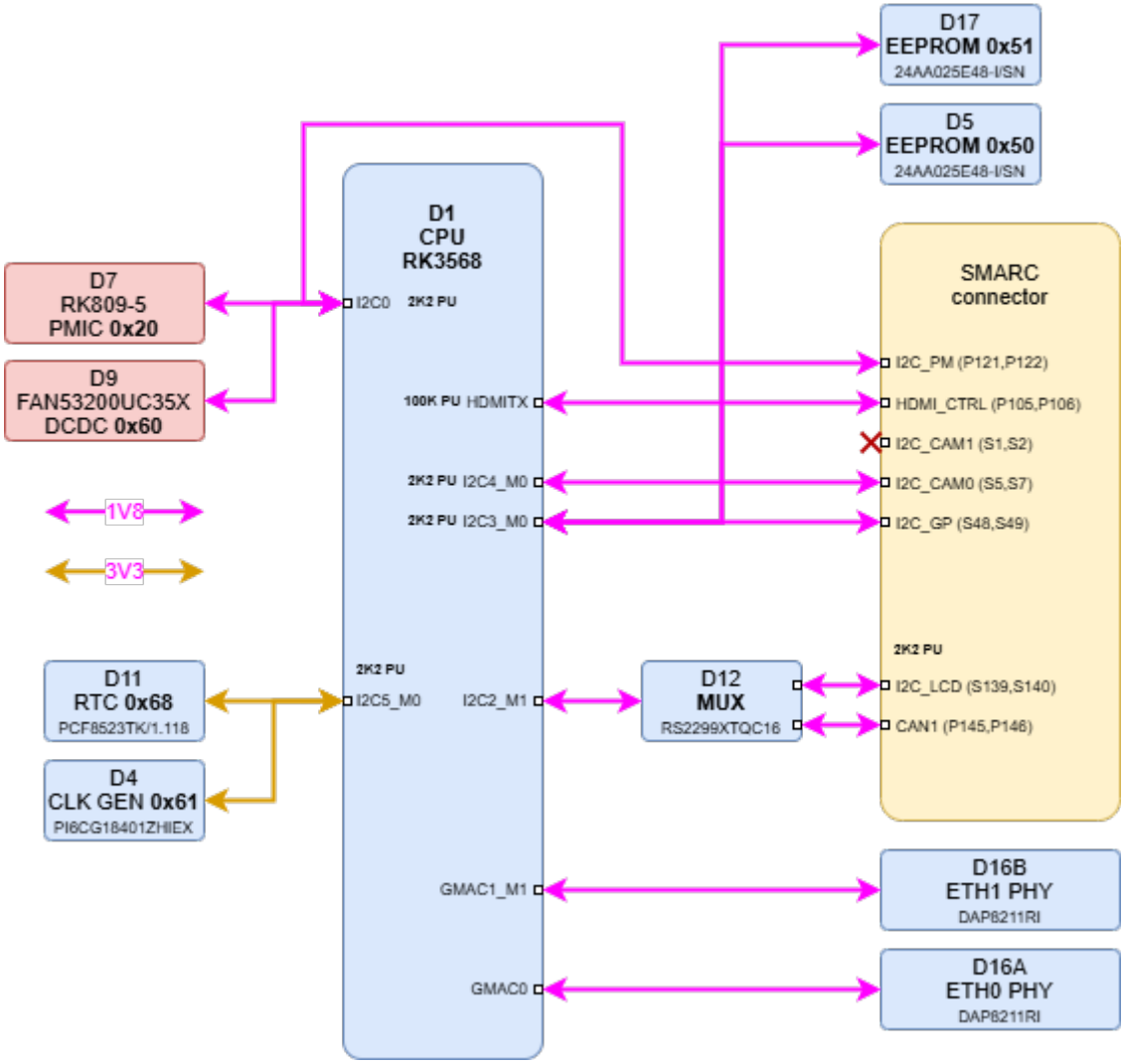


Рисунок 6: I2C интерфейс

Таблица 5: Сопоставление адресов I2C0

Устройство	**Адрес**
PMIC	0x00100000
DCDC CONV	0x01100000

Таблица 6: Сопоставление адресов I2C3

Устройство	**Адрес**
EEPROM 1 (D5)	0x01101000
EEPROM 2 (D17)	0x01100001

Таблица 7: Сопоставление адресов I2C5

Устройство	**Адрес**
RTC	0x01101000
CLK GEN	0x01100001

Расположение разъемов на плате

Вид сверху

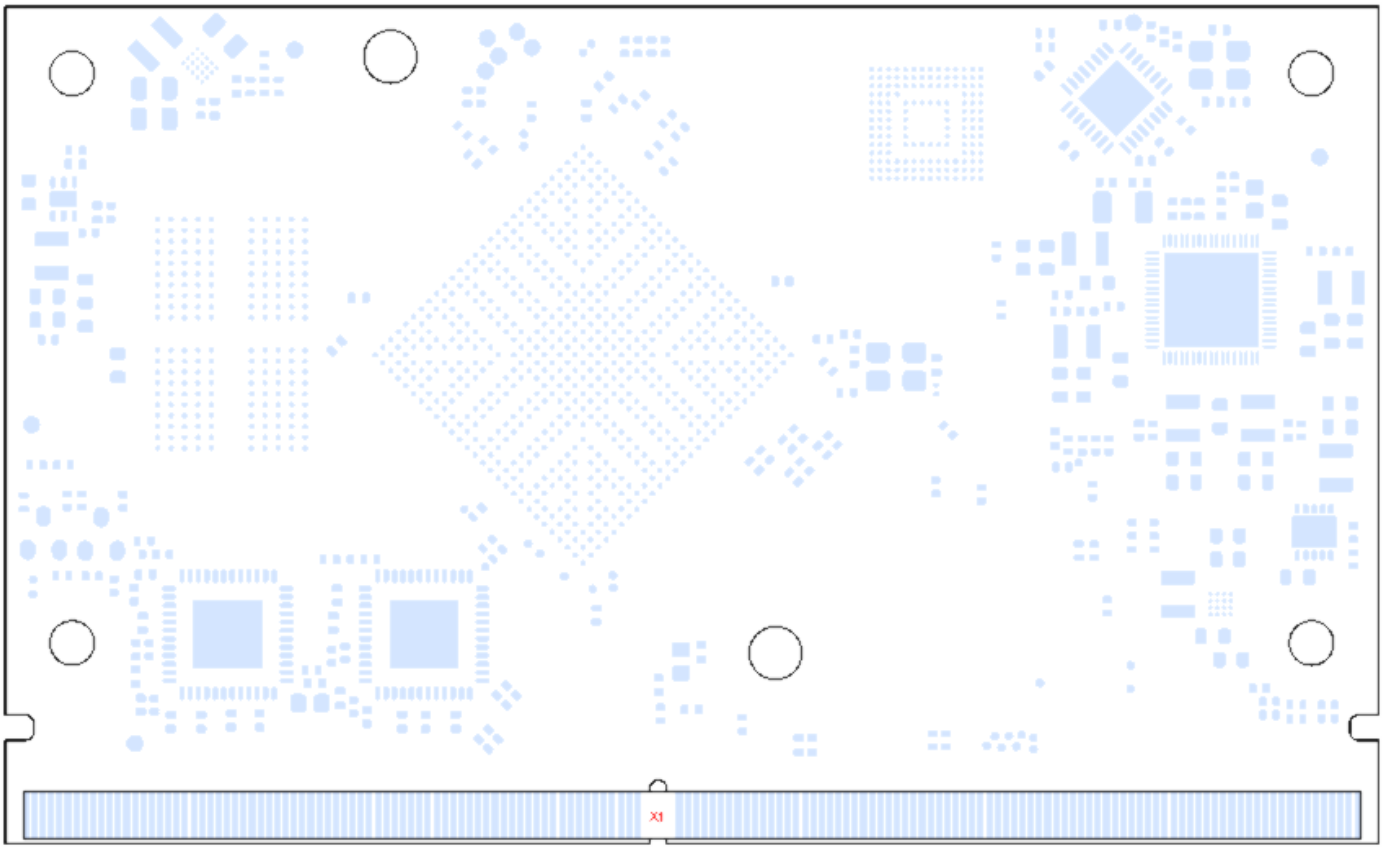


Рисунок 7: Расположение разъемов на плате. Вид сверху

Вид снизу

На нижней стороне платы разъемы отсутствуют.

Распиновка разъемов

Распиновка разъема X1 согласно SMARC

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P1	SMB_ALERT#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		SMBus Alert# (Interrupt) Signal	Standby/Sleep	
P2	GND	GND			PWR GND						
P3	CSI1_CK+	MIPI_CSI.CLK0._P	AG10	MIPI_CSI_RX_CLK 0P	CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	
P4	CSI1_CK-	MIPI_CSI.CLK0._N	AH10	MIPI_CSI_RX_CLK 0N	CSI1	I D-PHY			CSI1 differential clock input (point to point)	Runtime	
P5	GBE1_SDP	ETH1.SDP	-		GBE1	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P6	GBE0_SDP	ETH0.SDP	-		GBE0	I/O CMOS	3V3		IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	Standby	
P7	CSI1_RX0+	MIPI_CSI.0._P	AG12	MIPI_CSI_RX_D0P	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P8	CSI1_RX0-	MIPI_CSI.0._N	AH12	MIPI_CSI_RX_D0N	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P9	GND	GND			PWR GND						
P10	CSI1_RX1+	MIPI_CSI.1._P	AG11	MIPI_CSI_RX_D1P	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P11	CSI1_RX1-	MIPI_CSI.1._N	AH11	MIPI_CSI_RX_D1N	CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P12	GND	GND			PWR GND						
P13	CSI1_RX2+	**NC**	-		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P14	CSI1_RX2-	**NC**	-		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P15	GND	GND			PWR GND						
P16	CSI1_RX3+	**NC**	-		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P17	CSI1_RX3-	**NC**	-		CSI1	I D-PHY / I M-PHY			CSI1 differential input (point to point)	Runtime	
P18	GND	GND			PWR GND						
P19	GBE0_MDI3-	ETH0.MDI3._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P20	GBE0_MDI3+	ETH0.MDI3._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P21	GBE0_LINK100#	ETH0.LED_100#	-		GBE0	O OD CMOS	3V3	PU 10K	Link Speed Indication LED for GBE0 100Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
P22	GBE0_LINK1000#	ETH0.LED_1000#	-		GBE0	O OD CMOS	3V3	PU 10K	Link Speed Indication LED for GBE0 1000Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
P23	GBE0_MDI2-	ETH0.MDI2._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P24	GBE0_MDI2+	ETH0.MDI2._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P25	GBE0_LINK_ACT#	ETH0.LED_ACT#	-		GBE0	O OD CMOS	3V3	PU 10K	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	Shall be able to sink 24mA or more Carrier LED current.
P26	GBE0_MDI1-	ETH0.MDI1._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P27	GBE0_MDI1+	ETH0.MDI1._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P28	GBE0_CTREF	**NC**	-		GBE0	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
P29	GBE0_MDI0-	ETH0.MDI0._N	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P30	GBE0_MDI0+	ETH0.MDI0._P	-		GBE0	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
P31	SPI0_CS1#	SPI0.CS1	AD12	MIPI_DSI_TX1_D3P	SPI0	O CMOS	1V8		SPI0 Master Chip Select 1	Standby	
P32	GND	GND			PWR GND						
P33	SDIO_WP	SDIO_WP	AF25	GPIO0_A5_d SDMMC0_PWREN SATA_MP_SWITCH PCIE20_CLKREQn_M0	SDIO	I OD CMOS	1V8 or 3V3	PU 10K	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	Runtime	
P34	SDIO_CMD	SDMMC0.CMD	H27	GPIO2_A1_u SDMMC0_CMD PWM10_M1 UART5_RX_M0 CAN0_TX_M1	SDIO	I/O CMOS	1V8 or 3V3		SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	Runtime	
P35	SDIO_CD#	SDIO_CD#	Y22	GPIO0_A4_u SDMMC0_DET SATA_CP_DET PCIE30X1_CLKREQn_M0	SDIO	I OD CMOS	1V8 or 3V3	PU 10K	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	Runtime	
P36	SDIO_CK	SDMMC0.CLK	H28	GPIO2_A2_d SDMMC0_CLK TEST_CLKOUT UART5_TX_M0 CAN0_RX_M1	SDIO	O CMOS	1V8 or 3V3		SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	Runtime	SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
P37	SDIO_PWR_EN	SDIO_PWR_EN	-		SDIO	O CMOS	3V3		SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	Runtime	Should be driven low in Standby Mode by the Module. D1.AE24 (V1)
P38	GND	GND			PWR GND						
P39	SDIO_D0	SDMMC0.DATA.0	J25		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P40	SDIO_D1	SDMMC0.DATA.1	J24		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P41	SDIO_D2	SDMMC0.DATA.2	H26	GPIO1_D7_u SDMMC0_D2 ARMJTAG_TCK UART5_CTSn_M0	SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P42	SDIO_D3	SDMMC0.DATA.3	J23		SDIO	I/O CMOS	1V8 or 3V3		SDIO Data lines. These signals operate in push-pull mode.	Runtime	
P43	SPI0_CS0#	SPI0.CS0	AD20	GPIO0_C6_d PWM7_IR SPI0_CS0_M0 PCIE30X2_PERSTn_M0	SPI0	O CMOS	1V8		SPI0 Master Chip Select 0	Standby	This signal can be used to select Carrier SPI as boot device
P44	SPI0_CK	SPI0.SCK	AC22	GPIO0_B5_u I2C2_SCL_M0 SPI0_CLK_M0 PCIE20_WAKEn_M0 PWM1_M1	SPI0	O CMOS	1V8		SPI0 Clock	Standby	
P45	SPI0_DIN	SPI0.MISO	AC21	GPIO0_C5_d PWM6 SPI0_MISO_M0 PCIE30X2_WAKEn_M0	SPI0	I CMOS	1V8		SPI0 Master input / Slave output	Standby	also referred to as MISO

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P46	SPI0_DO	SPI0.MOSI	AA20	GPIO0_B6_u I2C2_SDA_M0 SPI0_MOSI_M0 PCIE20_PERSTn_M0 PWM2_M1	SPI0	O CMOS	1V8		SPI0 Master output / Slave input	Standby	also referred to as MOSI
P47	GND	GND			PWR GND						
P48	SATA_TX+	SATA1.D_TX._P	-		SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P49	SATA_TX-	SATA1.D_TX._N	-		SATA	O SATA			Serial ATA Channel 0 Transmit Output Differential Pair	Runtime	Series AC coupled on 10 nF Module
P50	GND	GND			PWR GND						
P51	SATA_RX+	SATA1.D_RX._P	-		SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P52	SATA_RX-	SATA1.D_RX._N	-		SATA	I SATA			Serial ATA Channel 0 Receive Input Differential Pair	Runtime	Series AC coupled on 10 nF Module
P53	GND	GND			PWR GND						
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	SPI1.CS0	AE8	GPIO4_C6_d PWM13_M1 SPI3_CS0_M1 SATA0_ACT_LED UART9_RX_M1 I2S3_SDI_M1	SPI1	O CMOS	1V8		SPI1 Master Chip Select 0	Standby	
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	SPI1.CS1	AH6	GPIO4_D1_u HDMITX_CEC_M0 SPI3_CS1_M1	SPI1	O CMOS	1V8		SPI1 Master Chip Select 1	Standby	
P56	ESPI_CK / SPI1_CK / QSPI_CK	SPI1.SCK	AF8	GPIO4_C2_d PWM14_M1 SPI3_CLK_M1 CAN1_RX_M1 PCIE30X2_CLKREQn_M2 I2S3_MCLK_M1	SPI1	O CMOS	1V8		SPI1 Clock	Standby	
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	SPI1.MISO	AD8	GPIO4_C5_d PWM12_M1 SPI3_MISO_M1 SATA1_ACT_LED UART9_TX_M1 I2S3_SDO_M1	SPI1	I CMOS	1V8		SPI1 Master input / Slave output	Standby	also referred to as MISO
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	SPI1.MOSI	AA11	GPIO4_C3_d PWM15_IR_M1 SPI3_MOSI_M1 CAN1_TX_M1 PCIE30X2_WAKEn_M2 I2S3_SCLK_M1	SPI1	O CMOS	1V8		SPI1 Master output / Slave input	Standby	also referred to as MOSI
P59	GND	GND			PWR GND						
P60	USB0+	USB2_HOST2._P	R2	USB2_HOST2_DP	USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P61	USB0-	USB2_HOST2._N	R1	USB2_HOST2_DM	USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P62	USB0_EN_OC#	USB2_HOST2_EN_OC#	AE5	GPIO3_A2_d LCDC_D9 VOP_BT1120_D1 GMAC1_TXD2_M0 I2S3_MCLK_M0 SDMMC2_D1_M1	USB0	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 0	Standby	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P63	USB0_VBUS_DET	**NC**	-		USB0	I USB VBUS 5V	USB VBUS 5V		USB Port 0 Host Power Detection	Standby	
P64	USB0_OTG_ID	**NC**	-		USB0				Input Pin to Announce OTG Device Insertion on USB 2.0 Port	Standby	
P65	USB1+	USB2_HOST3._P	T2	USB2_HOST3_DP	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P66	USB1-	USB2_HOST3._N	T1	USB2_HOST3_DM	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P67	USB1_EN_OC#	USB2_HOST3_EN_OC#	AG4	GPIO3_A3_d LCDC_D10 VOP_BT1120_D2 GMAC1_TXD3_M0 I2S3_SCLK_M0 SDMMC2_D2_M1	USB1	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 1	Standby	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P68	GND	GND			PWR GND						
P69	USB2+	USB3_HOST1._P	P24	USB3_HOST1_DP	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P70	USB2-	USB3_HOST1._N	P25	USB3_HOST1_DM	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P71	USB2_EN_OC#	USB3_HOST1_EN_OC#	AD2	GPIO3_C0_d LCDC_D23 PWM13_M0 GMAC1_MCLKINOUT_M0 UART3_RX_M1 PDM_SDI3_M2	USB2	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 2	Standby	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P72	RSVD	rsvd	-								
P73	RSVD	rsvd	-								
P74	USB3_EN_OC#	USB3_OTG0_EN_OC#	AH3	GPIO3_A5_d LCDC_D12 VOP_BT1120_D4 GMAC1_RXD3_M0 I2S3_SDO_M0 SDMMC2_CMD_M1	USB3	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 3	Standby	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P75	PCIE_A_RST#	PCIE_A_RST#	AB8	GPIO3_A1_d LCDC_D8 VOP_BT1120_D0 SPI1_CS0_M1 PCIE30X1_PERSTn_M1 SDMMC2_D0_M1	PCIEA	O CMOS	3V3		PCIe Port A reset output	Runtime	
P76	USB4_EN_OC#	**NC**	-		USB4	I/O OD CMOS	3V3		USB Over-Current Sense for Port 4	Standby	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P77	PCIE_B_CKREQ#	PCIE_B_CKREQ#	AF5	GPIO2_D4_d LCDC_D4 VOP_BT656_D4_M0 SPI2_CS1_M1 PCIE30X2_CLKREQn_M1 I2S1_SDI1_M2	PCIEB	IO OD CMOS	3V3	PU 10K	PCIe Port B clock request	Runtime	
P78	PCIE_A_CKREQ#	PCIE_A_CKREQ#	AC8	GPIO2_D2_d LCDC_D2 VOP_BT656_D2_M0 SPI0_CS0_M1 PCIE30X1_CLKREQn_M1 I2S1_LRCK_TX_M2	PCIEA	IO OD CMOS	3V3	PU 10K	PCIe Port A clock request	Runtime	
P79	GND	GND			PWR GND						
P80	PCIE_C_REFCK+	PCIE20_REFCLK._P	V24	PCIE20_REFCLKP	PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P81	PCIE_C_REFCK-	PCIE20_REFCLK._N	V25	PCIE20_REFCLKN	PCIEC	O PCIE			Differential PCIe Link C reference clock output	Runtime	
P82	GND	GND			PWR GND						
P83	PCIE_A_REFCK+	PCIE30_REFCLKA._P	-		PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	
P84	PCIE_A_REFCK-	PCIE30_REFCLKA._N	-		PCIEA	O PCIE			Differential PCIe Link A reference clock output	Runtime	
P85	GND	GND			PWR GND						
P86	PCIE_A_RX+	PCIE30_L0.D_RX._P	AC28	PCIE30_RX0P	PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P87	PCIE_A_RX-	PCIE30_L0.D_RX._N	AC27	PCIE30_RX0N	PCIEA	I PCIE			Differential PCIe link A receive data pair	Runtime	
P88	GND	GND			PWR GND						
P89	PCIE_A_TX+	PCIE30_L0.D_TX._P	AA28	PCIE30_TX0P	PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P90	PCIE_A_TX-	PCIE30_L0.D_TX._N	AA27	PCIE30_TX0N	PCIEA	O PCIE			Differential PCIe link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
P91	GND	GND			PWR GND						
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX.D2._P	AG22	HDMI_TX_D2P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX.D2._N	AH22	HDMI_TX_D2N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P94	GND	GND			PWR GND						
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX.D1._P	AG21	HDMI_TX_D1P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX.D1._N	AH21	HDMI_TX_D1N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P97	GND	GND			PWR GND						
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX.D0._P	AG20	HDMI_TX_D0P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX.D0._N	AH20	HDMI_TX_D0N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P100	GND	GND			PWR GND						
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX.CK._P	AH19	HDMI_TX_CLKP	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX.CK._N	AG19	HDMI_TX_CLKN	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P103	GND	GND			PWR GND						
P104	HDMI_HPD / DP1_HPD	HDMI_HPD	AB18	HDMI_TX_HPDIN	HDMI	I CMOS	1V8	PD 1M	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	Runtime	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_CTRL.SCL	AG8	GPIO4_C7_u HDMITX_SCL I2C5_SCL_M1	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_CLK Line Dedicated to HDMI	Runtime	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_CTRL.SDA	AG7	GPIO4_D0_u HDMITX_SDA I2C5_SDA_M1	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_DAT Line Dedicated to HDMI	Runtime	
P107	DP1_AUX_SEL	**NC**	-		DP1++_HDMI	I CMOS	1V8		Strapping Signal to Enable Either HDMI or DP Output	Runtime	0 - DP 1 - HDMI
P108	GPIO0 / CAM0_PWR#	GPIO.0	AA5	GPIO3_D5_d CIF_D7 EBC_SDDO7 SDMMC2_PWREN_M0 I2S1_SDI3_M1 VOP_BT656_D7_M1	GPIO	I/O CMOS	1V8		GPIO Pin 0 Preferred Output	Runtime	Shared with CAM0_PWR#
P109	GPIO1 / CAM1_PWR#	GPIO.1	AC1	GPIO3_D3_d CIF_D5 EBC_SDDO5 SDMMC2_CLK_M0 I2S1_SDI1_M1 VOP_BT656_D5_M1	GPIO	I/O CMOS	1V8		GPIO Pin 1 Preferred Output	Runtime	Shared with CAM1_PWR#
P110	GPIO2 / CAM0_RST#	GPIO.2	AA1	GPIO3_D4_d CIF_D6 EBC_SDDO6 SDMMC2_DET_M0 I2S1_SDI2_M1 VOP_BT656_D6_M1	GPIO	I/O CMOS	1V8		GPIO Pin 2 Preferred Output	Runtime	Shared with CAM0_RST#
P111	GPIO3 / CAM1_RST#	GPIO.3	Y7	GPIO3_D2_d CIF_D4 EBC_SDDO4 SDMMC2_CMD_M0 I2S1_SDI0_M1 VOP_BT656_D4_M1	GPIO	I/O CMOS	1V8		GPIO Pin 3 Preferred Output	Runtime	Shared with CAM1_RST#
P112	GPIO4 / HDA_RST#	GPIO.4	AB23	GPIO0_D4_d	GPIO	I/O CMOS	1V8		GPIO Pin 4 Preferred Output	Runtime	**NC (V2)**
P113	GPIO5 / PWM_OUT	GPIO.5	AH25	GPIO0_C7_d HDMITX_CEC_M1 PWM0_M1 UART0_CTSn	GPIO	I/O CMOS	1V8		GPIO Pin 5 Preferred Output	Runtime	**NC (V2)**
P114	GPIO6 / TACHIN	GPIO.6	G23	I2S2_MCLK_M0 ETH0_REFCLKO_25M UART7_RTSn_M0 SPI2_CLK_M0 GPIO2_C1_d	GPIO	I/O CMOS	1V8		GPIO Pin 6 Preferred Output	Runtime	**NC (V2)**
P115	GPIO7	GPIO.7	D20	I2S1_SDO1_M0 I2S1_SDI3_M0 PDM_SDI3_M0 PCIE20_CLKREQn_M2 ACODEC_DAC_DATAR GPIO1_B0_d	GPIO	I/O CMOS	1V8		GPIO Pin 7 Preferred Output	Runtime	**NC (V2)**
P116	GPIO8	GPIO.8	U2	CIF_CLKIN EBC_SDCLK GMAC1_MCLKINOUT_M1 UART1_CTSn_M1 I2S2_SCLK_RX_M1 GPIO4_C1_d	GPIO	I/O CMOS	1V8		GPIO Pin 8 Preferred Output	Runtime	**NC (V2)**
P117	GPIO9	GPIO.9	AB5	CIF_D2 EBC_SDDO2 SDMMC2_D2_M0 I2S1_LRCK_TX_M1 VOP_BT656_D2_M1 GPIO3_D0_d	GPIO	I/O CMOS	1V8		GPIO Pin 9 Preferred Output	Runtime	**NC (V2)**
P118	GPIO10	GPIO10	D23	GPIO1_D2_u FSPI_D0 FLASH_RDn	GPIO	I/O CMOS	1V8		GPIO Pin 10 Preferred Output	Runtime	**NC (V1)**
P119	GPIO11	GPIO11	A27	GPIO1_D4_u FSPI_D3 FLASH_CS1n	GPIO	I/O CMOS	1V8		GPIO Pin 11 Preferred Output	Runtime	**NC (V1)**
P120	GND	GND			PWR GND						

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P121	I2C_PM_CK	I2C_PM.SCL	AF24	GPIO0_B1_u I2C0_SCL	MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus CLK	Standby/Sleep	
P122	I2C_PM_DAT	I2C_PM.SDA	AB21	GPIO0_B2_u I2C0_SDA	MANAGEMENT	I/O OD CMOS	1V8	PU 2K2	Power management I2C bus DATA	Standby/Sleep	
P123	BOOT_SEL0#	BOOT.0	A24	GPIO1_B4_u EMMC_D0 FLASH_D0	BOOT	I OD CMOS	1V8	PU 10K	Input straps determine the Module boot device.	Standby	
P124	BOOT_SEL1#	**NC**	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P125	BOOT_SEL2#	**NC**	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P126	RESET_OUT#	RESET_OUT#	AC24	GPIO0_D6_d	MANAGEMENT	O CMOS	1V8		General purpose reset output to Carrier Board.	Standby	
P127	RESET_IN#	RESET_IN#	AH27	nPOR_u	MANAGEMENT	I OD CMOS	1V8...5V	PU 10K	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal Shall be level triggered during bootup to allow to stop booting of the module. After bootup it May act as an edge triggered signal.	Standby	
P128	POWER_BTN#	POWER_BTN#	-		MANAGEMENT	I OD CMOS	1V8...5V	PU 10K	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Sleep	
P129	SER0_TX	SER0.RXTX.TX	F26	GPIO2_C5_d I2S2_SDI_M0 GMAC0_RXER UART8_TX_M0 SPI2_CS1_M0	SER0	O CMOS	1V8		Asynchronous Serial Data Output Port 0	Runtime	
P130	SER0_RX	SER0.RXTX.RX	E26	GPIO2_C6_d CLK32K_OUT1 UART8_RX_M0 SPI1_CS1_M0	SER0	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 0	Runtime	
P131	SER0_RTS#	SER0.RTS	D26	GPIO2_B1_d SDMMC1_PWREN I2C4_SDA_M1 UART8_RTSn_M0 CAN2_RX_M1	SER0	O CMOS	1V8		Request to Send Handshake Line for Port 0	Runtime	
P132	SER0_CTS#	SER0.CTS	E25	GPIO2_B2_u SDMMC1_DET I2C4_SCL_M1 UART8_CTSn_M0 CAN2_TX_M1	SER0	I CMOS	1V8	PU 100K	Clear to Send Handshake Line for Port 0	Runtime	
P133	GND	GND			PWR GND						
P134	SER1_TX	SER1.TX	AH24	GPIO0_D1_u UART2_TX_M0	SER1	O CMOS	1V8		Asynchronous Serial Data Output Port 1	Runtime	
P135	SER1_RX	SER1.RX	AC20	GPIO0_D0_u UART2_RX_M0	SER1	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 1	Runtime	
P136	SER2_TX	SER2.RXTX.TX	AF2	GPIO3_B2_d LCDC_D17 VOP_BT1120_D8 GMAC1_RXD1_M0 UART4_TX_M1 PWM9_M0	SER2	O CMOS	1V8		Asynchronous Serial Data Output Port 2	Runtime	
P137	SER2_RX	SER2.RXTX.RX	AG1	GPIO3_B1_d LCDC_D16 VOP_BT1120_D7 GMAC1_RXD0_M0 UART4_RX_M1 PWM8_M0	SER2	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 2	Runtime	
P138	SER2_RTS#	**NC**	-		SER2	O CMOS	1V8		Request to Send Handshake Line for Port 2	Runtime	
P139	SER2_CTS#	**NC**	-		SER2	I CMOS	1V8		Clear to Send Handshake Line for Port 2	Runtime	
P140	SER3_TX	SER3.TX	AA7	GPIO3_C2_d LCDC_VSYNC VOP_BT1120_D14 SPI1_MISO_M1 UART5_TX_M1 I2S1_SDO3_M2	SER3	O CMOS	1V8		Asynchronous Serial Data Output Port 3	Runtime	
P141	SER3_RX	SER3.RX	AC4	GPIO3_C3_d LCDC_DEN VOP_BT1120_D15 SPI1_CLK_M1 UART5_RX_M1 I2S1_SCLK_RX_M	SER3	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 3	Runtime	
P142	GND	GND			PWR GND						

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P143	CAN0_TX	CAN0.TX	AG24	GPIO0_B3_u I2C1_SCL CAN0_TX_M0 PCIE30X1_BUTTONRSTn MCU_JTAG_TDO	CAN0	O CMOS	1V8		CAN Port 0 Transmit Output	Runtime	
P144	CAN0_RX	CAN0.RX	AB20	GPIO0_B4_u I2C1_SDA CAN0_RX_M0 PCIE20_BUTTONRSTn MCU_JTAG_TCK	CAN0	I CMOS	1V8		CAN Port 0 Receive Input	Runtime	
P145	CAN1_TX	CAN1.TX	V5	GPIO4_B5_d I2C2_SCL_M1 EBC_SDSHR CAN2_TX_M0 I2S1_SDO3_M1	CAN1	O CMOS	1V8		CAN Port 1 Transmit Output	Runtime	
P146	CAN1_RX	CAN1.RX	V6	GPIO4_B4_d I2C2_SDA_M1 EBC_GDSP CAN2_RX_M0 ISP_FLASH_TRIGIN VOP_BT656_CLK_M1	CAN1	I CMOS	1V8		CAN Port1 Receive Input	Runtime	
P147	VDD_IN	VDD_IN			PWR		3V...5.25V				
P148	VDD_IN	VDD_IN			PWR		3V...5.25V				
P149	VDD_IN	VDD_IN			PWR		3V...5.25V				
P150	VDD_IN	VDD_IN			PWR		3V...5.25V				
P151	VDD_IN	VDD_IN			PWR		3V...5.25V				
P152	VDD_IN	VDD_IN			PWR		3V...5.25V				
P153	VDD_IN	VDD_IN			PWR		3V...5.25V				
P154	VDD_IN	VDD_IN			PWR		3V...5.25V				
P155	VDD_IN	VDD_IN			PWR		3V...5.25V				
P156	VDD_IN	VDD_IN			PWR		3V...5.25V				
S1	CSI1_TX+ / I2C_CAM1_CK	**NC**	-		CSI1	I/O OD CMOS	1V8		I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0
S2	CSI1_TX- / I2C_CAM1_DAT	**NC**	-		CSI1	I/O OD CMOS	1V8		I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S3	GND	GND			PWR GND						
S4	RSVD	rsvd	-								
S5	CSI0_TX+ / I2C_CAM0_CK	I2C_CAM0.SCL	V1	GPIO4_B3_d I2C4_SCL_M0 EBC_GDOE ETH1_REFCLKO_25M_M1 SPI3_CLK_M0 I2S2_SDO_M1	CSI0	I/O OD CMOS	1V8	PU 2K2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2.0
S6	CAM_MCK	CAM_MCK	U3	GPIO4_C0_d CIF_CLKOUT EBC_GDCLK PWM11_IR_M1	CSI	O CMOS	1V8		Master clock output	Runtime	
S7	CSI0_TX- / I2C_CAM0_DAT	I2C_CAM0.SDA	V4	GPIO4_B2_d I2C4_SDA_M0 EBC_VCOM GMAC1_RXER_M1 SPI3_MOSI_M0 I2S2_SDI_M1	CSI0	I/O OD CMOS	1V8	PU 2K2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2.0
S8	CSI0_CK+	MIPI_CSI.CLK1._P	AG9	MIPI_CSI_RX_CLK1P	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S9	CSI0_CK-	MIPI_CSI.CLK1._N	AH9	MIPI_CSI_RX_CLK1N	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
S10	GND	GND			PWR GND						
S11	CSI0_RX0+	MIPI_CSI.2._P	AE11	MIPI_CSI_RX_D2P	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S12	CSI0_RX0-	MIPI_CSI.2._N	AD11	MIPI_CSI_RX_D2N	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S13	GND	GND			PWR GND						
S14	CSI0_RX1+	MIPI_CSI.3._P	AD9	MIPI_CSI_RX_D3P	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S15	CSI0_RX1-	MIPI_CSI.3._N	AE9	MIPI_CSI_RX_D3N	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
S16	GND	GND			PWR GND						
S17	GBE1_MDI0+	ETH1.MDI0._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S18	GBE1_MDI0-	ETH1.MDI0._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S19	GBE1_LINK100#	ETH1.LED_100#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 100Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
S20	GBE1_MDI1+	ETH1.MDI1._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S21	GBE1_MDI1-	ETH1.MDI1._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S22	GBE1_LINK1000#	ETH1.LED_1000#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 1000Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
S23	GBE1_MDI2+	ETH1.MDI2._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S24	GBE1_MDI2-	ETH1.MDI2._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S25	GND	GND			PWR GND						
S26	GBE1_MDI3+	ETH1.MDI3._P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S27	GBE1_MDI3-	ETH1.MDI3._N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
S28	GBE1_CTREF	**NC**	-		GBE1	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
S29	PCIE_D_TX+ / SERDES_0_TX+	**NC**	-		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S30	PCIE_D_TX- / SERDES_0_TX-	**NC**	-		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S31	GBE1_LINK_ACT#	ETH1.LED_ACT#	-		GBE1	O OD CMOS	3V3		Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	Shall be able to sink 24mA or more Carrier LED current.
S32	PCIE_D_RX+ / SERDES_0_RX+	**NC**	-		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S33	PCIE_D_RX- / SERDES_0_RX-	**NC**	-		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
S34	GND	GND			PWR GND						
S35	USB4+	**NC**	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S36	USB4-	**NC**	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
S37	USB3_VBUS_DET	USB3_VBUS_DET	M24	USB3_OTG0_VBUSDET	USB3	I USB VBUS 5V	USB VBUS 5V		USB Port 3 Host Power Detection	Standby	
S38	AUDIO_MCK	AUDIO_MCK	A19	GPIO1_A2_d I2S1_MCLK_M0 UART3_RTSn_M0 SCR_CLK PCIE30X1_PERSTn_M2	I2S	O CMOS	1V8		Master Clock Output to I2S Codec(s)	Runtime	
S39	I2S0_LRCK	I2S0.FS	A20	GPIO1_A5_d I2S1_LRCK_TX_M0 UART4_RTSn_M0 SCR_RST PCIE30X1_CLKREQn_M2 ACODEC_DAC_SYNK	I2S0	I/O CMOS	1V8		I2S0 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S40	I2S0_SDOUT	I2S0.DOUT	B20	GPIO1_A7_d I2S1_SDO0_M0 UART4_CTSn_M0 SCR_DET AUDIOPWM_ROUT_N ACODEC_DAC_DATAL	I2S0	O CMOS	1V8		I2S0 Digital Audio Output	Runtime	
S41	I2S0_SDIN	I2S0.DIN	B21	GPIO1_B3_d I2S1_SDI0_M0 PDM_SDI0_M0	I2S0	I CMOS	1V8		I2S0 Digital Audio Input	Runtime	
S42	I2S0_CK	I2S0.SCLK	B19	GPIO1_A3_d I2S1_SCLK_TX_M0 UART3_CTSn_M0 SCR_IO PCIE30X1_WAKEn_M2 ACODEC_DAC_CLK	I2S0	I/O CMOS	1V8		I2S0 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S43	ESPI_ALERT0#	**NC**	-		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	
S44	ESPI_ALERT1#	**NC**	-		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S45	MDIO_CLK	**NC**	-		SERDES	O CMOS	1V8		MDIO Signals to Configure Possible PHYs		
S46	MDIO_DAT	**NC**	-		SERDES	I/O OD CMOS	1V8		MDIO Signals to Configure Possible PHYs		
S47	GND	GND			PWR GND						
S48	I2C_GP_CK	I2C_GP.SCL	E18	GPIO1_A1_u I2C3_SCL_M0 UART3_TX_M0 CAN1_TX_M0 AUDIOPWM_LOUT_N ACODEC_ADC_CLK	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Clock Signal	Runtime	
S49	I2C_GP_DAT	I2C_GP.SDA	D18	GPIO1_A0_u I2C3_SDA_M0 UART3_RX_M0 CAN1_RX_M0 AUDIOPWM_LOUT_P ACODEC_ADC_DATA	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Data Signal	Runtime	
S50	HDA_SYNC / I2S2_LRCK	**NC**	-		I2S2	I/O CMOS	1V8		I2S2 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S51	HDA_SDO / I2S2_SDOUT	**NC**	-		I2S0	O CMOS	1V8		I2S2 Digital Audio Output	Runtime	
S52	HDA_SDI / I2S2_SDIN	**NC**	-		I2S0	I CMOS	1V8		I2S2 Digital Audio Input	Runtime	
S53	HDA_CK / I2S2_CK	**NC**	-		I2S0	I/O CMOS	1V8		I2S2 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S54	SATA_ACT#	**NC**	-		SATA	O OD CMOS	3V3		SATA Activity Indicator	Runtime	Shall be able to sink 24mA or more Carrier LED current
S55	USB5_EN_OC#	**NC**	-		USB5	I/O OD CMOS	3V3		USB Over-Current Sense for Port 5	Standby	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
S56	ESPI_IO_2 / QSPI_IO_2	**NC**	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S57	ESPI_IO_3 / QSPI_IO_3	**NC**	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S58	ESPI_RESET#	**NC**	-		eSPI	O CMOS	1V8		ESPI Reset	Standby	
S59	USB5+	**NC**	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S60	USB5-	**NC**	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S61	GND	GND			PWR GND						
S62	USB3_SSTX+	USB3_OTG0_SS.D_TX._P	T28	USB3_OTG0_SSTXP SATA0_TXP	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S63	USB3_SSTX-	USB3_OTG0_SS.D_TX._N	T27	USB3_OTG0_SSTXN SATA0_TXN	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S64	GND	GND			PWR GND						
S65	USB3_SSRX+	USB3_OTG0_SS.D_RX._P	R28	USB3_OTG0_SSRXP SATA0_RXP	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S66	USB3_SSRX-	USB3_OTG0_SS.D_RX._N	R27	USB3_OTG0_SSRXN SATA0_RXN	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S67	GND	GND			PWR GND						
S68	USB3+	USB3_OTG0._P	P27	USB3_OTG0_DP	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S69	USB3-	USB3_OTG0._N	P28	USB3_OTG0_DN	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S70	GND	GND			PWR GND						
S71	USB2_SSTX+	USB3_HOST1_SS.D_TX._P	V28	USB3_HOST1_SSTXP SATA1_TXP QSGMII_TXP_M0	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S72	USB2_SSTX-	USB3_HOST1_SS.D_TX._N	V27	USB3_HOST1_SSTXN SATA1_TXN QSGMII_TXN_M0	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S73	GND	GND			PWR GND						
S74	USB2_SSRX+	USB3_HOST1_SS.D_RX._P	U28	USB3_HOST1_SSRXP SATA1_RXP QSGMII_RXP_M0	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S75	USB2_SSRX-	USB3_HOST1_SS.D_RX._N	U27	USB3_HOST1_SSRXN SATA1_RXN QSGMII_RXN_M0	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S76	PCIE_B_RST#	PCIE_B_RST#	AD6	GPIO2_D6_d LCDC_D6 VOP_BT656_D6_M0 SPI2_MOSI_M1 PCIE30X2_PERSTn_M1 I2S1_SDI3_M2	PCIEB	O CMOS	3V3		PCIe Port B reset output	Runtime	
S77	PCIE_C_RST#	PCIE_C_RST#	AD1	GPIO3_C1_d LCDC_HSYNC VOP_BT1120_D13 SPI1_MOSI_M1 PCIE20_PERSTn_M1 I2S1_SDO2_M2	PCIEC	O CMOS	3V3		PCIe Port C reset output	Runtime	
S78	PCIE_C_RX+ / SERDES_1_RX+	PCIE20.D_RX._P	Y27	PCIE20_RXP SATA2_RXP QSGMII_RXP_M1	PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S79	PCIE_C_RX- / SERDES_1_RX-	PCIE20.D_RX._N	Y28	PCIE20_RXN SATA2_RXN QSGMII_RXN_M1	PCIEC	I PCIE			Differential PCIe link C receive data pair	Runtime	
S80	GND	GND			PWR GND						
S81	PCIE_C_TX+ / SERDES_1_TX+	PCIE20.D_TX._P	W27	PCIE20_TXP SATA2_TXP QSGMII_TXP_M1	PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S82	PCIE_C_TX- / SERDES_1_TX-	PCIE20.D_TX._N	W28	PCIE20_TXN SATA2_TXN QSGMII_TXN_M1	PCIEC	O PCIE			Differential PCIe link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S83	GND	GND			PWR GND						
S84	PCIE_B_REFCK+	PCIE30_REFCLKB._P	-		PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	
S85	PCIE_B_REFCK-	PCIE30_REFCLKB._N	-		PCIEB	O PCIE			Differential PCIe Link B reference clock output	Runtime	
S86	GND	GND			PWR GND						
S87	PCIE_B_RX+	PCIE30_L1.D_RX._P	AD28	PCIE30_RX1P	PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S88	PCIE_B_RX-	PCIE30_L1.D_RX._N	AD27	PCIE30_RX1N	PCIEB	I PCIE			Differential PCIe link B receive data pair	Runtime	
S89	GND	GND			PWR GND						
S90	PCIE_B_TX+	PCIE30_L1.D_TX._P	AB28	PCIE30_TX1P	PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S91	PCIE_B_TX-	PCIE30_L1.D_TX._N	AB27	PCIE30_TX1N	PCIEB	O PCIE			Differential PCIe link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
S92	GND	GND			PWR GND						
S93	DP0_LANE0+	EDP_TX.D0._P	J28	EDP_TX_D0P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S94	DP0_LANE0-	EDP_TX.D0._N	K27	EDP_TX_D0N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S95	DP0_AUX_SEL	**NC**	-		DP0++	I CMOS	1V8		Auxiliary Selection	Runtime	
S96	DP0_LANE1+	EDP_TX.D1._P	K28	EDP_TX_D1P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S97	DP0_LANE1-	EDP_TX.D1._N	L27	EDP_TX_D1N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S98	DP0_HPD	DP0_HPD	AG23	GPIO0_C2_d PWM3_IR EDP_HPDIN_M1 PCIE30X1_WAKEn_M0 MCU_JTAG_TMS	DP0++	I CMOS	1V8	PD 1M	DP Hot Plug Detect Input	Runtime	
S99	DP0_LANE2+	EDP_TX.D2._P	L28	EDP_TX_D2P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S100	DP0_LANE2-	EDP_TX.D2._N	M27	EDP_TX_D2N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S101	GND	GND			PWR GND						
S102	DP0_LANE3+	EDP_TX.D3._P	M28	EDP_TX_D3P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S103	DP0_LANE3-	EDP_TX.D3._N	N27	EDP_TX_D3N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S104	USB3_OTG_ID	USB3_OTG0_ID	L23	USB3_OTG0_ID	USB3	I CMOS	3V3		Input Pin to Announce OTG Device Insertion on USB 3.2 Port	Standby	
S105	DP0_AUX+	EDP_TX.AUX._P	L25	EDP_TX_AUXP	DP0++	I/O DP	3V3	PD 100K	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S106	DP0_AUX-	EDP_TX.AUX._N	M25	EDP_TX_AUXN	DP0++	I/O DP	3V3	PU 100K	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module. if DP0_AUX_SEL=1 (HDMI) - DC coupled
S107	LCD1_BKLT_EN	LCD1_BKLT_EN	AF23	GPIO0_C1_d PWM2_M0 NPUAVS UART0_TX MCU_JTAG_TDI	eDP1	O CMOS	1V8		Secondary LVDS Channel Backlight Enable	Runtime	
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	MIPI_DSI_TX1.4._P	AD15	MIPI_DSI_TX1_CLKP	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	MIPI_DSI_TX1.4._N	AE15	MIPI_DSI_TX1_CLKN	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S110	GND	GND			PWR GND						
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	MIPI_DSI_TX1.0._P	AD18	MIPI_DSI_TX1_D0P	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	MIPI_DSI_TX1.0._N	AE18	MIPI_DSI_TX1_D0N	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S113	eDP1_HPD / DSI1_TE	DSI1_TE	AB9	GPIO4_D2_d	DSI1	I CMOS	1V8		Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	Runtime	
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	MIPI_DSI_TX1.1._P	AD17	MIPI_DSI_TX1_D1P	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	MIPI_DSI_TX1.1._N	AC17	MIPI_DSI_TX1_D1N	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S116	LCD1_VDD_EN	LCD1_VDD_EN	AD22	GPIO0_C0_d PWM1_M0 GPUAVS UART0_RX	DSI1	O CMOS	1V8		Secondary Panel Power Enable	Runtime	
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	MIPI_DSI_TX1.2._P	AD14	MIPI_DSI_TX1_D2P	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	MIPI_DSI_TX1.2._N	AC14	MIPI_DSI_TX1_D2N	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S119	GND	GND			PWR GND						
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	MIPI_DSI_TX1.3._P	AD12	MIPI_DSI_TX1_D3P	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	MIPI_DSI_TX1.3._N	AE12	MIPI_DSI_TX1_D3N	DSI1	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S122	LCD1_BKLT_PWM	LCD1_BKLT_PWM	AH26	GPIO0_B7_d PWM0_M0 CPUAVS	DSI1	O CMOS	1V8		Secondary Panel Brightness Control	Runtime	
S123	GPIO13	GPIO.13	-		GPIO	I/O CMOS	1V8		GPIO Pin 13 Preferred Output	Runtime	**NC (V2)**
S124	GND	GND			PWR GND						
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSI_TX0_LVDS_TX0.0._P	AH17	MIPI_DSI_TX0_D0P LVDS_TX0_D0P	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSI_TX0_LVDS_TX0.0._N	AG17	MIPI_DSI_TX0_D0N LVDS_TX0_D0N	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	AD23	GPIO0_B0_u CLK32K_IN CLK32K_OUT0 PCIE30X2_BUTTONRSTn	DSI0	O CMOS	1V8		Primary Panel Backlight Enable	Runtime	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	MIPI_DSI_TX0_LVDS_TX0.1._P	AH16	MIPI_DSI_TX0_D1P LVDS_TX0_D1P	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	MIPI_DSI_TX0_LVDS_TX0.1._N	AG16	MIPI_DSI_TX0_D1N LVDS_TX0_D1N	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout

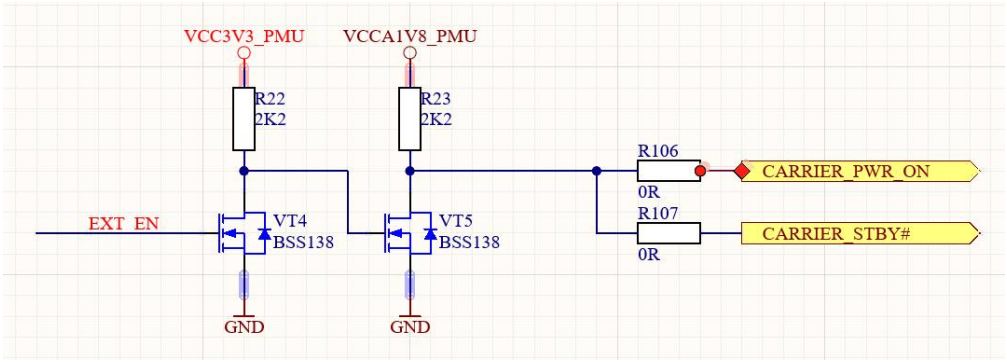
Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S130	GND	GND			PWR GND						
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSI_TX0_LVDS_TX0.2._P	AH14	MIPI_DSI_TX0_D2P LVDS_TX0_D2P	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	MIPI_DSI_TX0_LVDS_TX0.2._N	AG14	MIPI_DSI_TX0_D2N LVDS_TX0_D2N	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S133	LCD0_VDD_EN	LCD0_VDD_EN	AD25	GPIO0_D5_d	DSI0	O CMOS	1V8		Primary Panel Power Enable	Runtime	D1.AH25 (V2)
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	MIPI_DSI_TX0_LVDS_TX0.4._P	AH15	MIPI_DSI_TX0_CLKP LVDS_TX0_CLKP	DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	MIPI_DSI_TX0_LVDS_TX0.4._N	AG15	MIPI_DSI_TX0_CLKN LVDS_TX0_CLKN	DSI0	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S136	GND	GND			PWR GND						
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	MIPI_DSI_TX0_LVDS_TX0.3._P	AH13	MIPI_DSI_TX0_D3P LVDS_TX0_D3P	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	MIPI_DSI_TX0_LVDS_TX0.3._N	AG13	MIPI_DSI_TX0_D3N LVDS_TX0_D3N	DSI0	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Llayout
S139	I2C_LCD_CK	I2C_LCD.SCL	V5	GPIO4_B5_d I2C2_SCL_M1 EBC_SDSHR CAN2_TX_M0 I2S1_SDO3_M1	DSI	I\O OD CMOS	1V8	PU 2K2	I2C clock to read LCD display EDID EEPROMs	Runtime	
S140	I2C_LCD_DAT	I2C_LCD.SDA	V6	GPIO4_B4_d I2C2_SDA_M1 EBC_GDSP CAN2_RX_M0 ISP_FLASH_TRIGIN VOP_BT656_CLK_M1	DSI	I\O OD CMOS	1V8	PU 2K2	DDC Data Line Used for Flat Panel Detection and Control	Runtime	
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	AE23	GPIO0_C3_d PWM4 VOP_PWM_M0 PCIE30X1_PERSTn_M0 MCU_JTAG_TRSTn	DSI0	O CMOS	1V8		Primary Panel Brightness Control	Runtime	
S142	GPIO12	GPIO.12	-		GPIO	I/O CMOS	1V8		GPIO Pin 12 Preferred Output	Runtime	**NC (V2)**
S143	GND	GND			PWR GND						
S144	eDP0_HPD / DSI0_TE	DSI0_TE	AH7	GPIO4_C4_d EDP_HPDIN_M0 SPDIF_TX_M2 SATA2_ACT_LED PCIE30X2_PERSTn_M2 I2S3_LRCK_M1	DSI0	I CMOS	1V8		Primary DSI Panel Tearing Effect Signal	Runtime	
S145	WDT_TIME_OUT#	WDT_TIME_OUT#	C23	GPIO1_D3_u FSPI_CS0n FLASH_CS0n	WATCHDOG	O CMOS	1V8		Watch-Dog-Timer Output, low active	Runtime	
S146	PCIE_WAKE#	**NC**	-		PCIE	I OD CMOS	3V3		PCIe wake up interrupt to host – common to PCIe links A, B, C, D	Standby	
S147	VDD_RTC	VDD_RTC	-		PWR RTC		2V...3.25V				
S148	LID#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	Standby	
S149	SLEEP#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	Standby	
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	-		MANAGEMENT	I OD CMOS	VDD_IN	PU 10K	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.		

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S151	CHARGING#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	Standby/Sleep	
S152	CHARGER_PRSNT#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier if DC input for battery charger is present	Standby/Sleep	
S153	CARRIER_STBY#	CARRIER_STBY#	-		MANAGEMENT	O CMOS	1V8		The Module shall drive this signal low when the system is in a standby power state.	Standby	
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	-		MANAGEMENT	O CMOS	1V8		Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	Standby	
S155	FORCE_RECOV#	FORCE_RECOV#	B27	SARADC_VIN0	BOOT	I OD CMOS	1V8	PU 10K	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	Standby	
S156	BATLOW#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Battery low indication to Module. Carrier to float the line in inactive state.	Standby/Sleep	
S157	TEST#	**NC**	-		MANAGEMENT	I OD CMOS	1V8...5V		Held Low by Carrier to Invoke Module Vendor Specific Test Functions	Standby/Sleep	
S158	GND	GND			PWR GND						

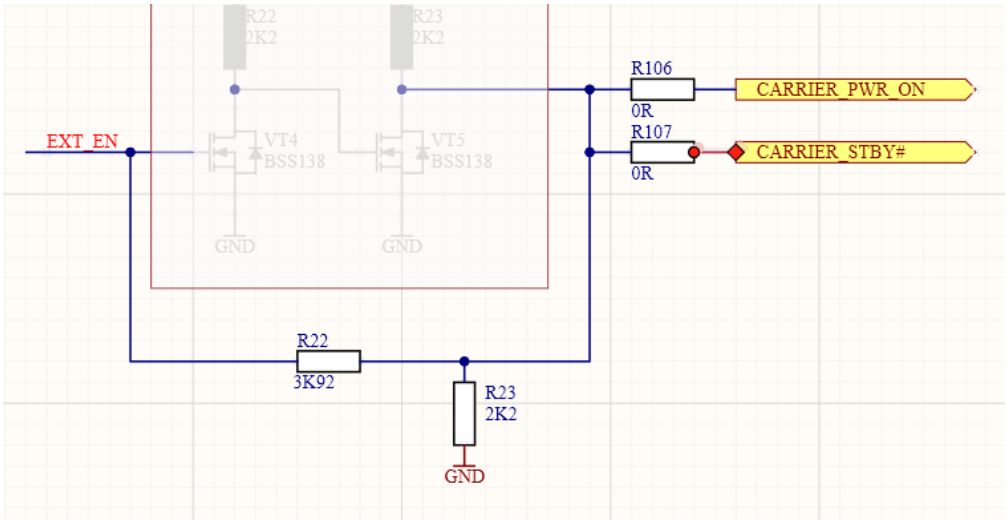
Отличия от NMS-SM-RK3568 v3 ds-ru

Сигналы CARRIER_PWR_ON и CARRIER_STBY# в V2, V3, V4 формируются PMIC; их состоянием нельзя управлять программно. В ревизии V3 инвертирование сигнала и преобразование уровня выполнялись транзисторной схемой. В ревизии V4 эти функции реализованы резистивной схемой.

Фрагмент схемы V3:

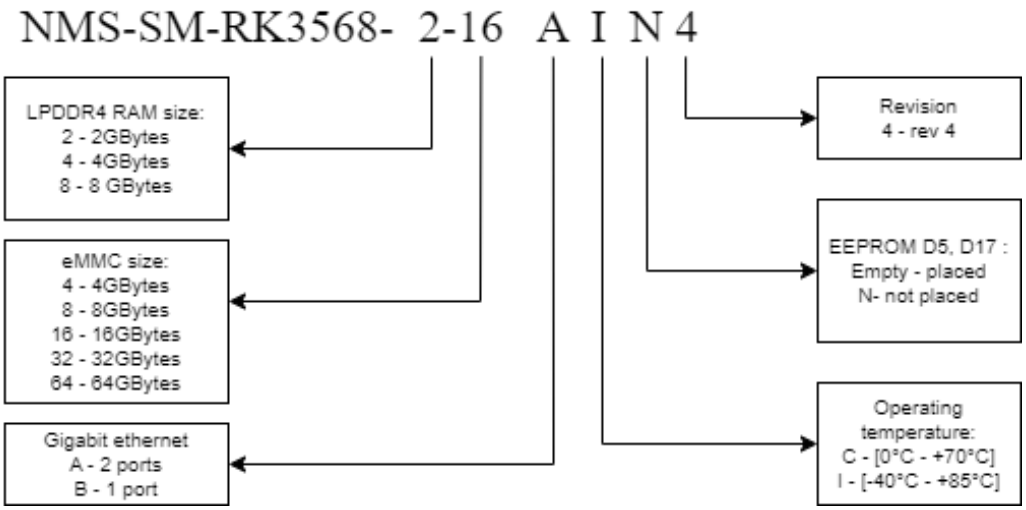


Фрагмент схемы для V4:



Замена логики была вызвана тем, что при отключении модуля питание 1V8_PMU остается активным для выполнения функций SLEEP-режима. А это приводило к тому, что подтяжка стока транзитора VT5 оставляла сигналы CARRIER_PWR_ON и CARRIER_STBY# всегда в логической единице.

Ordering information



NMS-SM-RK3568-2-64AI4	2 GBytes LPDDR4 RAM, 64 GBytes eMMC ROM, 2 Gigabit Ethernet (GBE0, GBE1), 2 EEPROM, Industrial
NMS-SM-RK3568-2-64AIN4	2 GBytes LPDDR4 RAM, 64 GBytes eMMC ROM, 2 Gigabit Ethernet (GBE0, GBE1), no EEPROM, Industrial